

Design and Implementation of 6-bit Charge Scaling Digital to Analog Converter (DAC) using 45 Nano-meter Technology

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Abstract---In this paper, The Design and Implementation of Charge Scaling Capacitor Digital to Analog Converter (DAC) in 45 nm technology using TANNER TOOL, V15 is presented. The simulation results show the transient analysis waveforms of charge scaling capacitor digital to analog convertor and also different blocks results . In charge scaling digital to analog convertor there is a capacitor and operational amplifier used and also switch is used. The switch is make from CMOS transmission gate which is used for the on and off time in charge scaling capacitor DAC. Here the DAC logic is used for the feedback and its made from the charge scaling capacitor. This design is for low power and low area consumption in chip or circuit design and compared with each other. These charge scaling DAC is high speed switching and low power consumption with compares to any other DAC.

Keywords: CMOS, Op-Amp, Switch, DAC Logic, TANNER TOOL

I. INTRODUCTION

In an analog to digital system the quality of the digital signal is main criteria, for long distance transmission it is necessary to convert analog signal into digital signal at input side, same as convert digital signal into analog signal at output side. CMOS technologies have been used for low power applications; also submicron processes have allowed CMOS to achieve low power. In this paper charge scaling capacitor digital to analog convertor using 45nm technology are presented. The block diagram of charge scaling capacitor DAC is shown below:

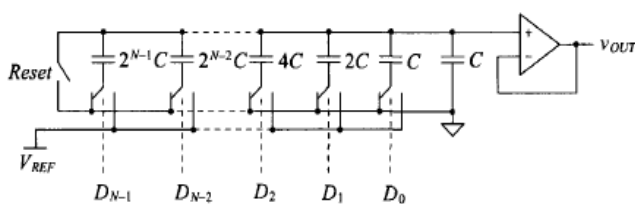


Fig. 1: Block Diagram of charge scaling DAC

Hera a charge scaling DAC is convert the digital waveform into analog. In this block diagram as shown the capacitor and operational amplifier is used for the conversions of signal. Here the operational amplifier is for the give result of analog output and for the on-off time the transmission gate based CMOS switch is used and then it give to the capacitor. The one input of op-amp is give from the capacitor ladder and another is form the feedback of it. So that finally the analog output is occur.

II. CHARGE SCALING DAC

One of the most common implementations of the successive approximation ADC, the charge-redistribution successive

approximation ADC, uses a charge scaling DAC. The charge scaling DAC simply consists of an array of individually switched binary-weighted capacitors. The amount of charge upon each capacitor in the array is used to perform the aforementioned binary search in conjunction with a comparator internal to the DAC and the successive approximation register.

- (1) First, the capacitor array is completely discharged to the offset voltage of the comparator, V_{OS} . This step provides automatic offset cancellation(i.e. The offset voltage represents nothing but dead charge which can't be juggled by the capacitors).
- (2) Next, all of the capacitors within the array are switched to the input signal, v_{IN} . The capacitors now have a charge equal to their respective capacitance times the input voltage minus the offset voltage upon each of them.
- (3) In the third step, the capacitors are then switched so that this charge is applied across the comparator's input, creating a comparator input voltage equal to $-v_{IN}$.
- (4) Finally, the actual conversion process proceeds. First, the MSB capacitor is switched to V_{REF} , which corresponds to the full-scale range of the ADC. Due to the binary-weighting of the array the MSB capacitor forms a 1:1 charge divider with the rest of the array. Thus, the input voltage to the comparator is now $-v_{IN}$ plus $V_{REF}/2$. Subsequently, if v_{IN} is greater than $V_{REF}/2$ then the comparator outputs a digital 1 as the MSB, otherwise it outputs a digital 0 as the MSB. Each capacitor is tested in the same manner until the comparator input voltage converges to the offset voltage, or at least as close as possible given the resolution of the DAC.

A very popular DAC architecture used in CMOS technology is the charge-scaling DAC. Fig, a parallel array of binary-weighted capacitors, totaling $2NC$, is connected to an op-amp. The value, C , is a unit capacitance of any value. After initially being discharged, the digital signal switches each capacitor to either V^{\wedge} or ground, causing the output voltage, v_{OUT} , to be a function of the voltage division between the capacitors.

The capacitor array totals $2NC$. Therefore, if the MSB is high and the remaining bits are low, then a voltage divider occurs between the MSB capacitor and the rest of the array. The analog output voltage, v_{OUT} , becomes

$$v_{OUT} = V_{REF} \cdot \frac{2^{N-1}C}{(2^{N-1} + 2^{N-2} + 2^{N-3} + \dots + 4 + 2 + 1)C} = V_{REF} \cdot \frac{2^{N-1}C}{2^N C} = \frac{V_{REF}}{2}$$

which confirms the fact that the MSB changes the output of a DAC by $1/2 V_{REF}$. Figure shows the equivalent circuit under this condition. The ratio between v_{OUT} and V^{\wedge} due to each capacitor can be generalized to

$$V_{OUT} = \frac{2^k C}{2^N C} \cdot V_{REF} = 2^{k-N} \cdot V_{REF}$$

where it is assumed that the k -th bit, D_k , is one and all other bits are zero. Superposition can then be used to find the value of V_{OUT} for any digital input word by

$$V_{OUT} = \sum_{k=0}^{N-1} D_k 2^{k-N} \cdot V_{REF}$$

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

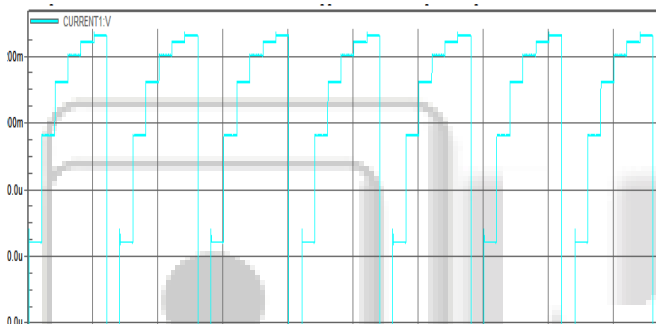


Fig. 2: Result of 6-bit charge scaling DAC

One limitation of this architecture is the existence of a parasitic capacitance at the top plate of the capacitor array due to the op-amp. This will prohibit its use as a high-resolution data converter. A better implementation would include the use of a parasitic insensitive, switched-capacitor integrator as the driving circuit.

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