Design and Simulation of 2GHz Current Starved VCO for Frequency Synthesizer

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Abstract—A low power 2GHz CSVCO is presented in this paper for PLL Frequency synthesizer. The current starved VCO is used to decrease power consumption and to improve noise characteristic of the synthesizer. The proposed VCO achieves low phase noise and wide tuning range and consume low power. The measured noise phase is –44.77 dBc/Hz at 1 MHz offset. The operating frequency can be tuned from 5.231 MHz-5.098 GHz with the supply voltage varying from 0.1 V to 1V step of 0.5 mV. Therefore, wide the tuning range is achieved. The center frequency of VCO is 2 GHz at 0.5V approximately. The VCO circuit, dissipated 47.874 µW power under a 1V supply voltage. The VCO is design and simulated on Tanner EDA Tool using 45nm CMOS process technology with supply voltage 1 V.

Keywords: Phase locked loop (PLL), Current Starved Voltage control oscillator (VCO), Complementary metal oxide semiconductor (CMOS), Tanner Tool.

I. INTRODUCTION

Wireless communication systems contain low-noise amplifiers, mixers, power amplifiers, and phase-locked loops (PLLs). In particular, the PLL, which provides the function of frequency synthesis, is very important in designing such systems. The voltage-controlled oscillator (VCO) often plays the key element in PLL circuit. Designing VCO for the monolithic integration is always desirable but most challenging. In general, there are two main structures of designing the VCO in monolithic integration. One is the LC-based integrated oscillator and the other is the ring oscillator. The low phase noise, wide tuning range, and low power dissipation and are the most important factors of the basic design of a VCO. The operations of the LC oscillators are excellent in phase-noise performance but their tuning ranges are only about 10% to 20% [1-3]. Besides, they often require extra processes and occupy a large area of chip size due to the existence of inductor and capacitor. However, the ring oscillators have wide tuning range and low power dissipation.

The paper is organized as follows: section II, presents some details on the VCO architecture and its design. In section III, the simulation results of the VCO implementation are shown and discussed. Conclusions are given in the last section.

II. CURRENT STARVED VCO

A. CSVCO overview

The current-starved VCO is shown schematically in Fig.1 [5]. Its operation is similar to the ring oscillator discussed earlier. MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for current. The drain currents of MOSFETs M5 and M6 are the same, and are set by the input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage. The filter configurations we have discussed rely on the fact that the input resistance of the VCO is practically infinite and the input capacitance is small compared to the capacitances present in the loop filter. Attaining infinite input resistance is usually an easy part of the design. For the charge-pump configuration, the input capacitance of the VCO can be added to C2. To determine the design equations for use with the current-starved VCO, consider the simplified schematic of one stage of the VCO shown in Fig.1. The total capacitance on the drains of M2 and M3 is given by

\[ C_{tot} = C_{out} + C_{in} \]  

(1)

This is simply the output and input capacitances of the inverter. This equation can be written in a more useful form as

\[ C_{tot} = (3/2) C'_{ox} (W_{pLp} + W_{nLn}) \]  

(2)

The time it takes to charge \( C_{tot} \) from zero to VSP with the constant-current \( I_d \) is given by

\[ t_1 = C_{tot} (V_{sp}/I_d) \]  

(4)

While the time it takes to discharge \( C_{tot} \) from VDD to VSP is given by

\[ t_2 = \frac{C_{tot}(V_{DD} - V_{sp})}{I_d} \]  

(5)

If we set \( I_d = I_d = I_{center} \) which we will label \( I_{center} \) when \( V_{in} = VDD/2 \), then the sum of \( t_1 \) and \( t_2 \) is simply

\[ I_1 + I_2 = (C_{tot} V_{DD})/I_d \]  

(6)

The oscillation frequency of the current-starved VCO for \( N \) (an odd number > 5) of stages is

\[ f_{osc} = \frac{1}{N(t_1 + t_2)} \]

(7)

\[ = \frac{1}{ID} \]

Which is = \( f_{center} \) when \( V_{in} = VDD/2 \) and \( ID = I_{center} \)
B. Design of VCO

- **VCO specification:**

  \[
  \begin{align*}
  VDD & = 1V, \\
  t_{ox} & = 14A^0, \\
  \varepsilon_0 & = 8.85aF/μm, \\
  \varepsilon_r & = 3.97, \\
  I_D & = 10μA, \\
  f_{osc} & = 2GHz, \\
  L_n & = L_p = 1, \\
  W_n & = 10, W_p = 20.
  \end{align*}
  \]

  We begin by calculating the total capacitance \( C'_{ox} \).

  \[
  C'_{ox} = \frac{C_{ox}}{\varepsilon_0 \varepsilon_r} = \frac{25fF/μm^2}{2}
  \]

  Using equation (3) and assuming the inverter \( M_2,M_3 \) are sized equal for drive, that is,

  \[
  C_{tot} = \frac{5}{2} \cdot C'_{ox} \cdot (W_pL_p + W_nL_n)
  \]

  \[
  = \frac{5}{2} \cdot 25fF/μm^2 \cdot (10 \cdot 1 + 20 \cdot 1) \cdot (0.045 \mu m)^2
  = 3.7fF
  \]

  Let’s use a center drain current of 10μA based on \( I_d-V_{gs} \)
  characteristics of the MOSFETs. The selection of the current
  is important because when \( V_{invco} = VDD/2 \), the oscillation
  to be 2.4GHz.

  The number of stages, using equation (7), is given by

  \[
  N = \frac{I_D}{VDD \cdot C_{tot} \cdot f_{osc}}
  \]

  \[
  = \frac{10μA}{2GHz \cdot 3.7fF \cdot 1V}
  = 5
  \]

  Total 5 stages are required to generate 2GHz oscillation
  frequency at the control voltage of approximately \( VDD/2 \).

III. Simulation Result of Current Starved VCO

Schematic view of current starved VCO is shown in
following figure 2. VCO consist of 5 stage.

The transient analysis of current starved VCO is shown
in figure 3. For input control voltage, \( V_{invco} \), equal to 0.50mV,
an output frequency of 2.4GHz has been obtained. The input
control voltage is varied from 0.1V to 1V, in steps of
0.5V, and output Frequency is observed.

<table>
<thead>
<tr>
<th>Input voltage (Vincco)</th>
<th>Frequency (MHz)</th>
<th>Power Dissipation (μW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.10</td>
<td>5.231</td>
<td>0.5279</td>
</tr>
<tr>
<td>0.15</td>
<td>14.123</td>
<td>1.317</td>
</tr>
<tr>
<td>0.20</td>
<td>38.861</td>
<td>0.4637</td>
</tr>
<tr>
<td>0.25</td>
<td>102.408</td>
<td>1.317</td>
</tr>
<tr>
<td>0.30</td>
<td>248.963</td>
<td>3.526</td>
</tr>
</tbody>
</table>
Table 1: Relation between control Voltage, \( V_{\text{invco}} \) and oscillation Frequency

<table>
<thead>
<tr>
<th>( V_{\text{invco}} ) (mV)</th>
<th>( F_{\text{max}} ) (MHz)</th>
<th>( F_{\text{min}} ) (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.35</td>
<td>558.459</td>
<td>8.692</td>
</tr>
<tr>
<td>0.40</td>
<td>1090.84</td>
<td>18.778</td>
</tr>
<tr>
<td>0.45</td>
<td>1741.618</td>
<td>32.883</td>
</tr>
<tr>
<td>0.50</td>
<td>2006.12</td>
<td>45.230</td>
</tr>
<tr>
<td>0.53</td>
<td>2400.34</td>
<td>47.847</td>
</tr>
<tr>
<td>0.55</td>
<td>3086.59</td>
<td>60.964</td>
</tr>
<tr>
<td>0.60</td>
<td>3650.06</td>
<td>71.900</td>
</tr>
<tr>
<td>0.65</td>
<td>4139.857</td>
<td>80.673</td>
</tr>
<tr>
<td>0.70</td>
<td>4481.209</td>
<td>86.821</td>
</tr>
<tr>
<td>0.75</td>
<td>4673.737</td>
<td>93.414</td>
</tr>
<tr>
<td>0.80</td>
<td>4921.158</td>
<td>95.278</td>
</tr>
<tr>
<td>0.85</td>
<td>5054.57</td>
<td>97.450</td>
</tr>
<tr>
<td>0.90</td>
<td>5000.15</td>
<td>96.535</td>
</tr>
<tr>
<td>0.95</td>
<td>5098.692</td>
<td>98.318</td>
</tr>
</tbody>
</table>

The gain of the VCO is calculated from the table 1 is given by

\[ K_{\text{vco}} = \frac{2\pi \times (F_{\text{max}} - F_{\text{min}})}{V_{\text{max}} - V_{\text{min}}} \text{ (radian/s*V)} \]

\[ = \frac{2\pi \times (4.82 \times 10^{-10} - 40.32 \times 10^{-6})}{0.8 - 0.2} \]

Therefore gain is

\[ K_{\text{vco}} = 5 \times 10^{-10} \text{ (radian/s*V)} \]

From table 1, the measured tuning range of the VCO is 5.23MHz to 5098MHz. As shown in figure 3.3 the plot of the input control voltage versus the output oscillation frequency. It shows that 2.4GHz frequency is obtained at \( V_{\text{invco}} \) equal to 0.50mV.

![Plot of VCO vs Frequency](image)

**Fig. 4:** Plot of oscillation frequency versus control voltage

The figure 5 shows the output frequency spectrum of the VCO with center frequency at 2GHz for \( V_{\text{invco}} \) of 0.5mV. The power dissipation at the center frequency of 2.4GHz for the input control voltage 0.50mV is 47.874µW.

![Output Frequency Spectrum](image)

**Fig. 5:** Output Frequency Spectrum of VCO

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Table 2: CSVCO Performance Summary

<table>
<thead>
<tr>
<th>Specification</th>
<th>Simulation Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>45nm</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1V</td>
</tr>
<tr>
<td>VCO tuning rang</td>
<td>5.231MHz-5.098GHz</td>
</tr>
<tr>
<td>Center Frequency</td>
<td>2.006GHz</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-44.77dBc/Hz</td>
</tr>
</tbody>
</table>

Table 3: Comparison of SCVCO with other paper
REFERENCES


