Design and Simulation of 2GHz Current Starved VCO for Frequency Synthesizer

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Abstract—A low power 2GHz CSVCO is presented in this paper for PLL Frequency synthesizer. The current starve VCO is used to decrease power consumption and to improve noise characteristic of the synthesizer. The proposed VCO achieves low phase noise and wide tuning range and consume low power. The measured phase noise is –44.77dBc/Hz at 1 MHz offset. The operating frequency can be tuned from 5.231MHz-5.098GHz with the supply voltage varying from 0.1 V to 1V step of 0.5mV. Therefore, wide the tuning range is achieved. The canter frequency of VCO is 2GHZ at 0.5V approximately. The VCO circuit, dissipated 47.874µW power under a 1V supply voltage. The VCO is design and simulated on Tanner EDA Tool using 45nm CMOS process technology with supply voltage 1 V.

Keywords: Phase locked loop (PLL), Current Starved Voltage control oscillator (VCO), Complementary metal oxide semiconductor (CMOS), Tanner Tool.

I. INTRODUCTION

Wireless communication systems contain low-noise amplifiers, mixers, power amplifiers, and phase-locked loops (PLLs). In particular, the PLL, which provides the function of frequency synthesis, is very important in de-signing such systems. The voltage-controlled oscillator (VCO) often plays the key element in PLL circuit. De-signing VCO for the monolithic integration is always desirable but most challenging. In general, there are two main structures of designing the VCO in monolithic integration. One is the LC-based integrated oscillator and the other is the ring oscillator. The low phase noise, wide tuning range, and low power dissipation and are the most important factors of the basic design of a VCO. The operations of the LC oscillators are excellent in phase-noise performance but their tuning ranges are only about 10% to 20% [1-3]. Besides, they often require extra processes and occupy a large area of chip size due to the existence of inductor and capacitor. However, the ring oscillators have wide tuning range and low power dissipation.

The paper is organized as follows: section II, presents some details on the VCO architecture and its design. In section III, the simulation results of the VCO implementation are shown and discussed. Conclusions are given in the last section.

II. CURRENT STARVED VCO

A. *CSVCO overview*

The current-starved VCO is shown schematically in Fig.1 [5].Its operation is similar to the ring oscillator discussed earlier. MOSFETs M2 and M3 operate as an inverter, while MOSFETs Ml and M4 operate as current sources. The current sources, Ml and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for current. The drain currents of MOSFETs M5 and M6 are the same and are set by the input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage. The filter configurations we have discussed rely on the fact that the input resistance of the VCO is practically infinite and the input capacitance is small compared to the capacitances present in the loop filter. Attaining infinite input resistance is usually an easy part of the design. For the charge-pump configuration, the input capacitance of the VCO can be added to C2. To determine the design equations for use with the current-starved VCO, consider the simplified schematic of one stage of the VCO shown in Fig.1. The total capacitance on the drains of M2 and M3 is given by

$$C_{tot} = C_{out} + C_{in} \quad (1)$$

$$C_{tot} = C'_{ox}(W_pL_p + W_{,,}L_n) + (3/2)\,C'_{ox}(W_pL_p + W_nL_n) \quad (2)$$

This is simply the output and input capacitances of the inverter. This equation can be written in a more useful form as

$$C_{tot} = (5/2)\,C'_{ox}(W_pL_p + W_nL_n) \quad (3)$$

The time it takes to charge Ctot from zero to VSP with the constant-current Id is given by

$$t_1 = C_{tot}(V_{sp}/I_{D4}) \quad (4)$$

While the time it takes to discharge Ctot from VDD to Vsp is given by

$$t_2 = \frac{C_{tot}(VDD - V_{sp}}{ID_1} \quad (5)$$

If we set $I_{D4} = I_D = I_D$ (which we will label IDcenter when VinVC0 = VDD/2), then the sum of t1 and t2 is simply

$$t_1 + t_2 = (C_{tot} * VDD)/I_D \quad (6)$$

The oscillation frequency of the current-starved VCO for N (an odd number > 5) of stages is

$$f_{osc} = \frac{1}{N(t1+t2)} = \frac{ID}{N \bullet Ctot \bullet VDD} \quad (7)$$

Which is =fcenter (@VinVCO = VDD/2 and ID = IDcenter)

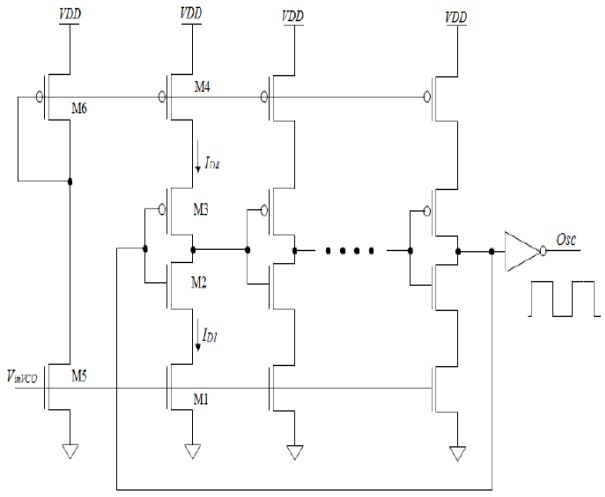

Fig. 1: Current starved VCO

B. Design of VCO

- *VCO specification:*

VDD=1V,
t_{ox} = 14A^0 ,
ε_0 = 8.85aF/μm,
ε_r = 3.97,
I_D = 10μA,
fosc = 2GHz,
L_n = Lp = 1,
W_n = 10, W_p = 20.
We begin by calculating the total capacitance C'$_{ox}$.

$$C'_{ox} = \frac{\varepsilon ox}{tox} = \frac{\varepsilon o\, \varepsilon r}{tox} = 25fF/\mu m^2 \quad (8)$$

Using equation (3) and assuming the inverter ,M2,M3 are sized equal for drive, that is ,

$$C_{tot} = \frac{5}{2} \bullet C'_{ox} (WpLp+WnLn) \quad (9)$$

$$= \frac{5}{2} \bullet 25\frac{fF}{\mu m2} \bullet (10 \bullet 1+20 \bullet 1) \bullet (0.045\ \mu m)^2$$

$$= 3.7fF$$

Let's use a center drain current of 10μA based on Id-Vgs characteristics of the MOSFETs. The selection of the current is important because when Vinvco is VDD/2, the oscillation to be 2.4GHz.
The number of stages, using equation (7), is given by

$$N = \frac{ID}{VDD \bullet Ctot \bullet fosc} \quad (10)$$

$$= \frac{10\mu A}{2GHz \bullet 3.7fF \bullet 1V}$$

= 5
Total 5 stages are required to generate 2GHz oscillation frequency at the control voltage of approximately VDD/2.

III. Simulation Result of Current Starved VCO

Schematic view of current starved VCO is shown in following figure 2.VCO consist of 5 stage.

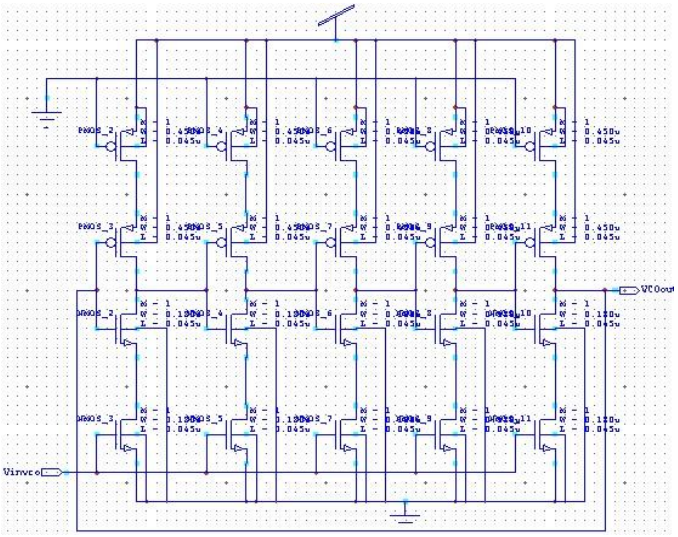

Fig 2.Current starved VCO

The transient analysis of current starved VCO is shown in figure 3.For input control voltage, Vinvco, equal to 0.50mV, an output frequency of 2.4GHz has been obtained. The input control voltage is varied from 0.1V to 1V,in steps of 0.5V,and output Frequency is observed.

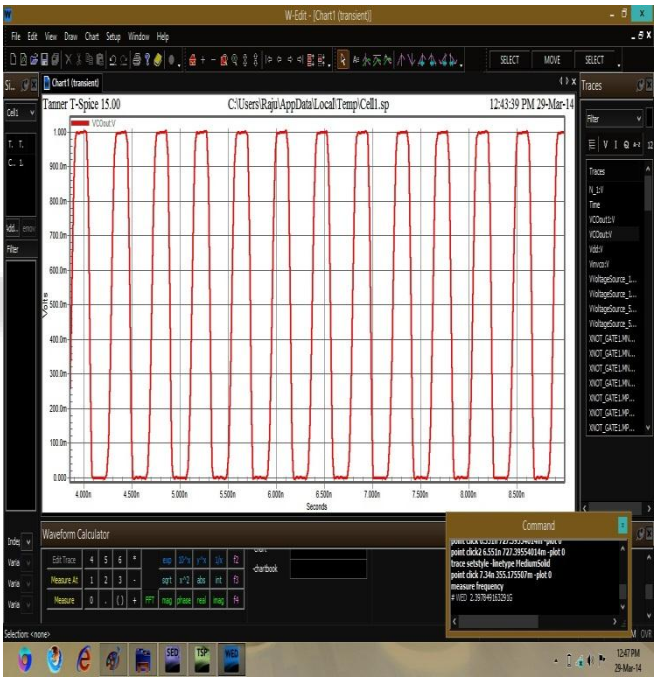

Fig. 3: Output Waveform of Current Starved VCO at Vinvco = 0.50mv

The table 1 shows relationship between input control voltage, Vinvco, of the VCO and the output Oscillation frequency of the VCO. In table 3.1 frequency and power dissipation at different values of the input control voltages has been calculated.

Input voltage (Vinvco)	Frequency (MHz)	Power Dissipation (μW)
0.10	5.231	0.5279
0.15	14.123	0.1572
0.20	38.861	0.4637
0.25	102.408	1.317
0.30	248.963	3.526

0.35	558.459	8.692
0.40	1090.84	18.778
0.45	1741.618	32.833
0.50	2006.12	45.230
0.53	2400.34	47.874
0.55	3086.59	60.964
0.60	3650.06	71.900
0.65	4139.857	80.673
0.70	4481.209	86.821
0.75	4673.737	90.801
0.80	4821.158	93.414
0.85	4923.323	95.212
0.90	5000.15	96.535
0.95	5054.57	97.540
1	5098.692	98.318

Table. 1: Relation between control Voltage, Vinvco and oscillation Frequency

The gain of the VCO is calculated from the table 1 is given by

$$K_{vco} = 2\pi \times \frac{(F_{max}-F_{min})}{V_{max} - V_{min}} \quad \text{(radian/s*V)}$$

$$= \frac{2\pi\times(4.82\times10\times10\hat{}9-40.32\times10\times10\hat{}6)}{0.8-0.2}$$

Therefore gain is

K_{vco} =5×10 ^10 (radian/s*V)

From table1, the measured tuning range of the VCO is 5.23MHz to5098MHz. As shown in figure 3.3 the plot of the input control voltage versus the output oscillation frequency. It shows that 2.4GHz frequency is obtain at Vinvco equal to 0.50mV.

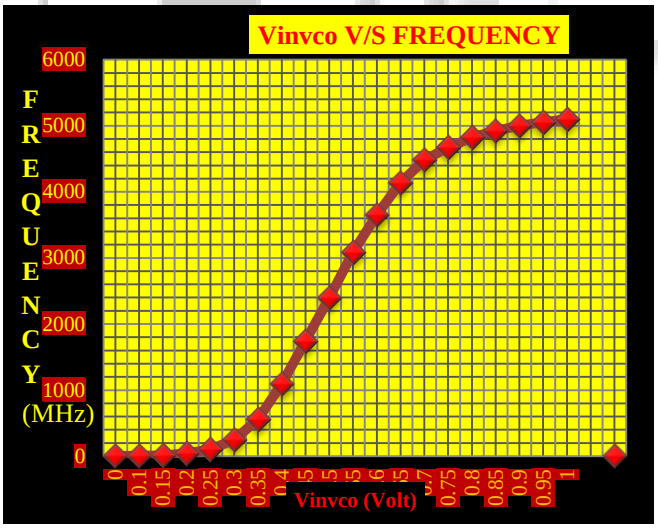

Fig. 4: Plot of oscillation frequency versus control voltage

The figure 5 shows the output frequency spectrum of the VCO with center frequency of 2.4GHz for input control voltage of 0.53mV.The power dissipation at the center frequency of 2.4GHz for the input control voltage o.50mv is 47.874µW.

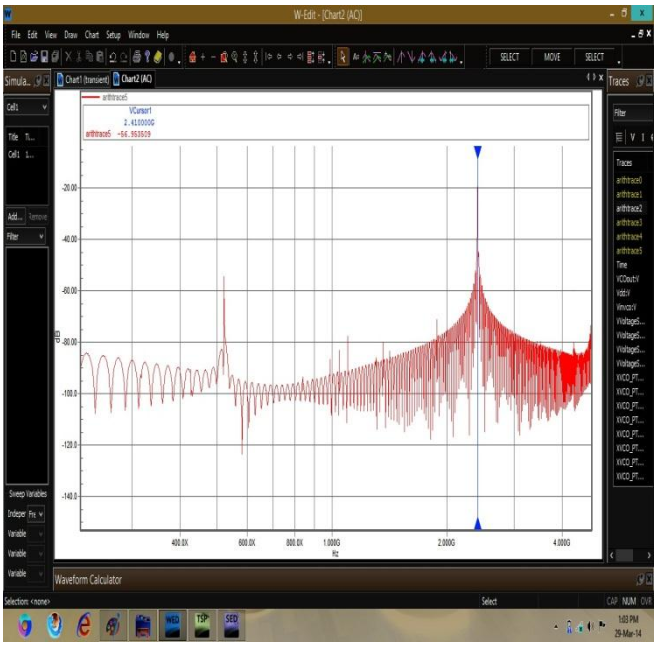

Fig. 5: Output Frequency Spectrum of VCO

Specification	Simulation Result
Technology	45nm
Supply voltage	1V
VCO tuning rang	5.231MHz-5.098GHz
Center Frequency	2.006GHz
Phase Noise	-44.77dB/Hz

Table. 2 : CSVCO Performance Summary

IV. CONCLUSION

A low power current starved VCO has been presented for PLL Frequency synthesizer. The design has been simulated in a standard 45nm CMOS technology. The VCO generates a center frequency at 2GHz at Vinco of 0.5mV approximately.The measured tuning range of VCO is 2.46GHz-2.541GHz with the supply voltage varying from 0.1 V to 1V step of 0.5mV.The measured phase noise is -44.77 dBc/Hz at 1 MHz offset and the power consumption is 47.874µW.

Parameters	**Result of current work**	**Results Reported in [1]**		**Results Reported in [2]**
Technology	45nm	45nm	65nm	90nm
Supply voltage	1V	1.1V	1.2V	-
Frequency Rang.	5.231MHz-5.098GHz	1.2 -2.4 GHz	3.5 – 5GHz	0.432GHz
Phase Noise	-44.77dBc/Hz	-95dBc/Hz @1MHz	-119dBc/Hz @1MHz	-102dBc/Hz
Power Dissipation	47.874µW	5.4mw	1.2mw	7mw

Table. 3 : Comparison of SCVCO with other paper

REFERENCES

[1] Seok-Ju Yun, Kwi-Dong Kim, and Jong-Kee Kwon "A Low-Spur CMOS PLL Using Differential Compensation Scheme". ETRI Journal, August 2012, Number 4, Volume 34.
[2] Te-Wen Liao, Jun-Ren Su, and Chung-Chih Hung, "Ring-VCO Based Low Noise and Low Spur Frequency Synthesizer" , IEEE 2013,pp.1861-1864.
[3] Sehmi Saad, Mongia Mhiri, Aymen Ben Hammadi, "A CMOS 0.35-µm, 3.3-V PLL Synthesizer for Bluetooth Transmitter", International Conference on Design & Technology of Integrated Systems in Nanoscale Era,2012 IEEE
[4] C. C. Boon 1, M.Vamshi Krishna 2," A 1.2 V 2.4 GHz Low Spur CMOS PLL Synthesizer with a gain boosted Charge Pump for a Batteryless Transceiver", 2012 IEEE International Symposium on Radio-Frequency Integration Technology.pp.222-224.
[5] R. Jacob Baker. "CMOS circuit design, layout, and simulation". Second Edition 2002, ISBN-978-81-265-2037-4.
[6] Sung-mo kang,Yusuf leblabici. "CMOS digital integrated circuit analysis and disign".3rd Edition.

