Transmitter Module of 10Gb/s Ethernet MAC

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Abstract--- 10 Gb Ethernet is part of the IEEE 802.3 standard. It is also faster version of the Ethernet where half duplex operation mode is not supported. This design is based on Xilinx LogiCORE 10-Gigabit Ethernet MAC in which transmitter and receiver module are separately designed. Therefore the transmit engine will be specifically designed to interface the client and the physical layer.
Keywords: Ethernet MAC transmitter, Xilinx LogiCORE

I. INTRODUCTION

10 Gb/s Ethernet MAC is used to interface to physical layer device into high speed Ethernet system. The 10GE MAC core is designed to the IEEE 802.3 standard specification and supports the high bandwidth demands of network IP traffic on WAN, LAN and MAN [3]. This system design is compatible to work with Virtex®-6, Virtex-5 and Virtex-4 and Virtex-II Pro and Spartan®-6 platforms.

The Xilinx 10GEMAC core is another of the SystemIO solutions which provide high performance inter connects technologies for communications equipment and flexibility in implementing emerging interface standards. The MAC core performs the Link function of the 10 Gb Ethernet standard. The 10 Gigabit Media Independent Interface (XGMII) version of this core is intended to interface to either an off-chip PHY device or XAUI LogiCORE using the XGMII Interface.

This core design can be also attached to the XAUI core. Due to this pin count can be reduced as well as we can improve operating distance. These are the advantages of using XAUI rather than XGMII interface. XGMII interface is omitted from 10Gb Ethernet MAC core at customization time. XAUI core is interfaced by internal FPGAs [4]. This case is shown in Fig 2.

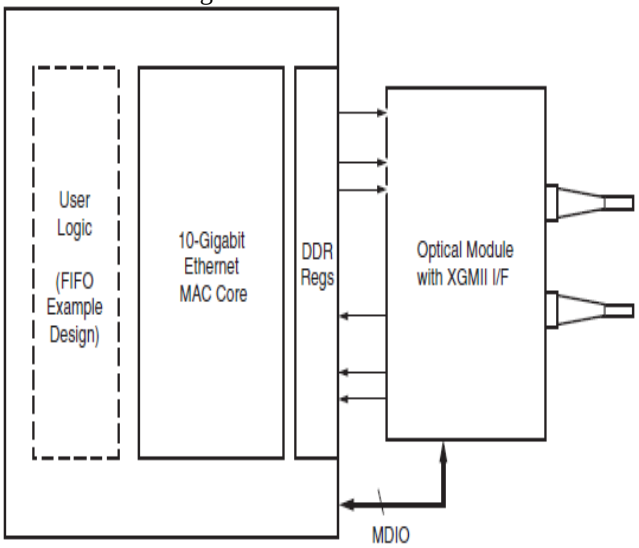

Fig. 1: Core is connected to PHY with XGMII

II. SYSTEM DESIGN

10Gb Ethernet MAC core includes functions like interface with user logic, flow control, reconciliation sublayer, XGMII interface connections, management interface, statistic Counters and MIDO.

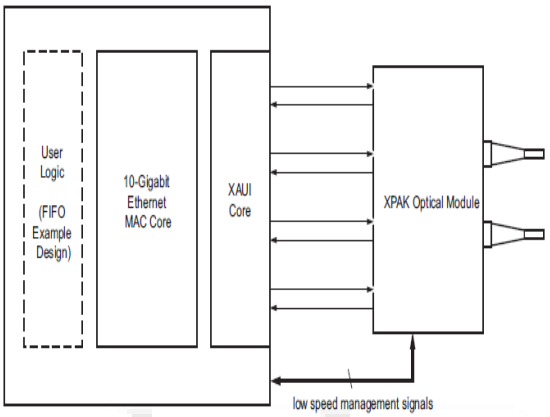

Fig. 2: 10-Gigabit Ethernet MAC Core Used with Xilinx XAUI Core [4]

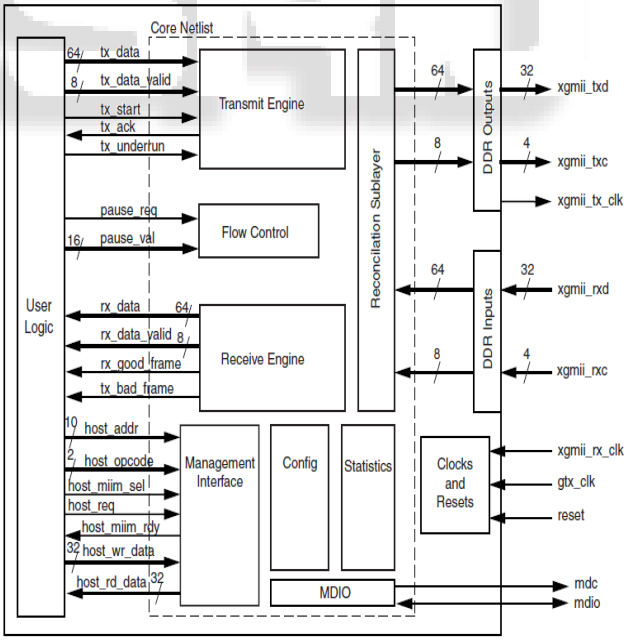

Fig. 3: Block diagram of 10Gb Ethernet MAC core [4]

Data flow can be divided into transmit process and receive process.

A. Transmit process:

a) Data Frame: Get data from user logic (contains DA, SA, and DATA) from user logic. Transmit Engine module computes PAD, adds SFD and PRE characters,

and append FCS (if it is not provided by user logic), then package the data into packaged MAC frame.

b) Control Frame: To get pause data (time to pause receiver's transmitting process) from user logic. Flow Control module put trans MAC control frame (contains broadcast address, SA, L/T, and pause data) to Transmit Engine Module. Transmit Engine module computes PAD, adds SFD and PRE characters, and appends FCS (if it is not provided by user logic), then package the data into packaged MAC frame.

B. Receive process:

a) Data Frame: To get received MAC frame (DA, SA, L/T, DATA and FCS) from RS module. To check FCS and DA fields, send data to logic (DA, SA, L/T, DATA and FCS) to user logic and indicate if data to logic is good or bad.

b) Control Frame: To get received MAC frame (DA, SA, L/T, DATA and FCS) from RS module and recognize it as a MAC Control Frame.

Flow Control module sends corresponding pause operation to Transmit Engine.

III. TRANSMITTER MODULE DESIGN

The transmit engine provides the interface between the client and physical layer. Fig 4 shows a block diagram of the transmit engine with the interfaces to the client, physical, management and the flow control.

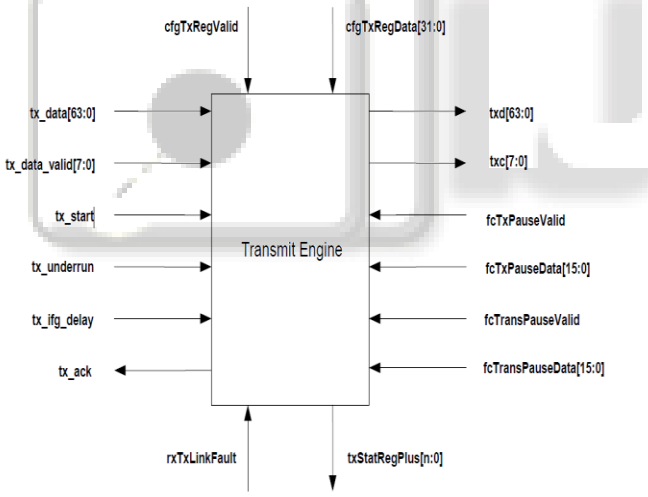

Fig. 4: Block diagram of transmitter engine

The transmit engine contains several blocks; input and output FIFO/register, control logic and counters. The input and output FIFO or registers are employing to receive data from the client and distribute the data to the physical. All data flow is all under controlled from the control logic.

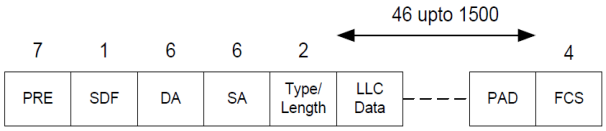

Fig. 5: IEEE 802.3x frame

Above Fig shows the standard MAC frame used for transmitting to the physical [1]. Preamble has a value of 10101010 and the SFD has a value of 10101011. The tx_ack signal is generated using a type of counter circuitry to compensate when paused frame transmission is invoked by the flow control block or the inter frame delay is set at the start. The assertion of the signal is achieve when the count equal to the delay value. The request from the pause or inter frame will used to select the counter delay value. The minimum inter frame gap is 96 bits. For a normal transmission, the delay value will be 2 clock cycles.

The control logic is essentially a state machine that controls how the data is output to the physical by selecting between the control bytes and the client data. There are four different states in the control logic and there are IDLE, START, DATA and PAUSE.

In the IDLE state, IDLE bytes (07) are transmitted to the physical. When a receive fault occurs, the state machine will be stuck at IDLE until the signal is de-asserted.

In the START state, START control bytes, PREAMBLE bytes and Start Frame Delimiter are loaded into the output. Once the data is loaded, the state changed to DATA.

In the DATA state, the FIFO empty 64 bits at a time to the output until the empty flag is set. In this state, the tx_data_valid bytes are inverted and output to the command output, txc. If the empty flag is asserted in any of the FIFO, the output register with no valid data will be loaded with the TERMINATE and IDLE control bytes. After the last frame is transmitted, the state machine will either change to the IDLE state or when fcTransPauseVal signal is asserted, the state machine will change to the PAUSE state.

In the PAUSE state, a pause frame is sent out to the physical. In this state, the tx_ack is delayed until the pause frame is transmitted. The tx_ack signal is used to indicate to the client that the first data column is received.

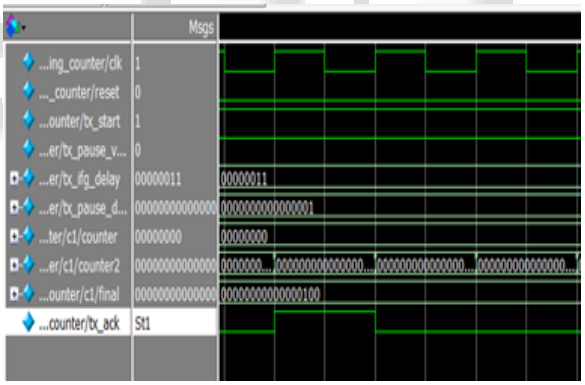

Fig. 6: Acknowledgement granted

When the tx_underrun is asserted by the client-side, an error code will be inserted to the frame transmission.

When VLAN is enabled, the transmitter is able to accept VLAN frames. The VLAN ID has a value of 8100 and the total frame size if extended to 1522 bytes.

When FCS is required for the data from the client, a parallel scheme is employed to generate the FCS. If the data is less than 46 bytes, padding is applied to the appropriate FIFO or registers. This is only achieved when the length of frame is received.

The length will indicate if the frame is below the minimum frame size. By knowing the size, the appropriate FIFO or register can be applied with the padding. If the frame is greater than the maximum size, a counter is used to track the number of data columns and using the length field, this will determine when to truncate the data. An error code will be inserted to the transmission to corrupt the frame.

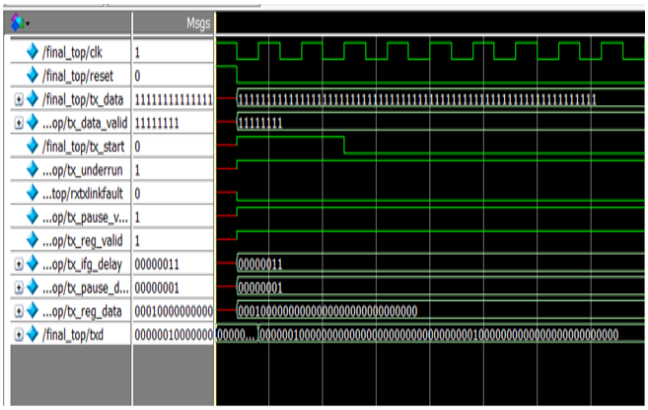

Fig. 7: Error Frame when Underrun

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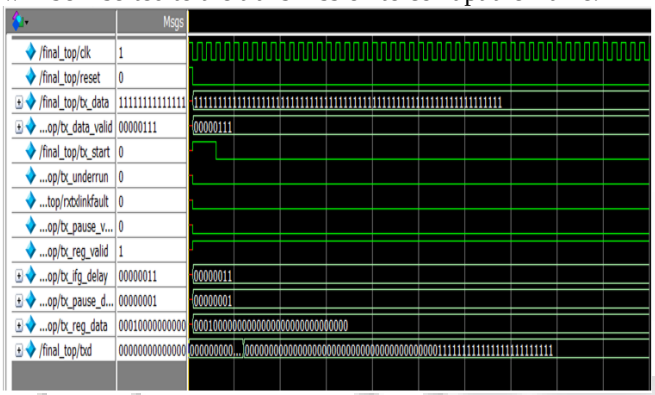

Fig. 8: Data Transfer with 3 LSB register valid case

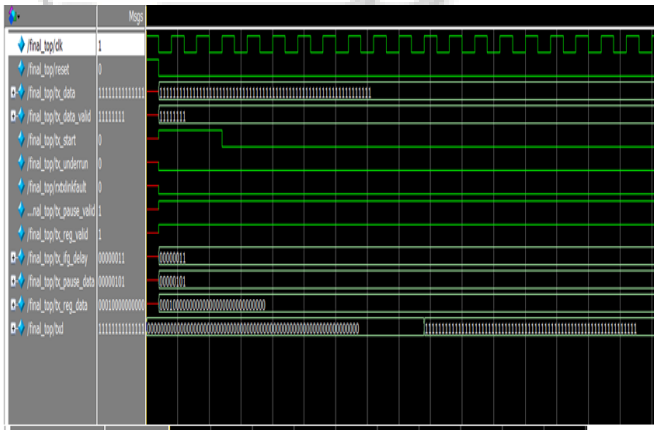

Fig. 9: Data Transfer with all register valid case with pausing the acknowledgment

IV. FSM FOR NORMAL TRANSMISSION WITH FCS SUPPLIED

State machine description

IDLE: continue transmitting IDLEs until tx_ack is received.

START: transmit the first64 bit data. This includes start control byte, six preambles and Start Frame Delimiter.

DATA: Load data from FIFO. Also check when tx_data_valid is equal to zero, load terminates and IDLE bytes at the appropriate section.

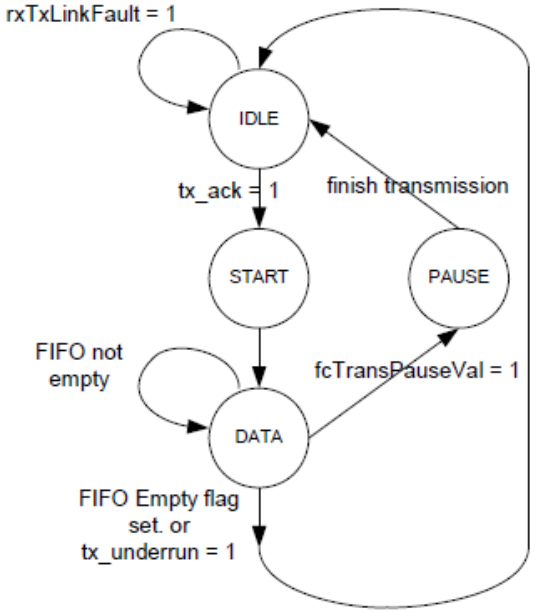

Fig. 10: FSM for transmission process

PAUSE: Transmit PAUSE Frame.

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