A New Dual Stack Transistor for Ground Bounce and Leakage Current Reduction

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Abstract---In this paper the author have discussed the trade-off between current CMOS technology scaling and static power consumption issues. This power consumption is an important concern for designing a low power integrated circuit. This paper has discussed different approaches for a low power integrated circuit design using leakage power reduction techniques. The main focus is on dual stack power gating approach which reduces the leakage power near about 75% in comparison to base design without the power gating structure at 90 nm technology.

I. INTRODUCTION

The current progress in semiconductor industry has increased many aspect of designing the portable and other electronic devices. This progress has increased the chip density, operating frequency and most important unwanted property is increment in power dissipation [2]. The chip density has increased because of the miniaturization of semiconductor technology. There are so many factors which affect the power dissipation; one of the most unintentional is leakage power dissipation. This leakage occurs when device functional blocks are in off state. This leakage power phenomenon occurs all because of the transistor scaling [2, 3]. As the feature size down , shorter channel length result in increased sub threshold leakage current through transistor when it is off, because of these reasons, static power consumption. The other cause of power consumption is also a ground bounce noise [2, 3]. This phenomenon comes into existence when an excessive voltage transfers through a ground wire connection with higher frequency. There are so many techniques which has been discussed for leakage and ground bounce reduction [3].We have proposed a new approach using dual stack of transistors in 90 nm technology and some of the previous work has been discussed with our power gating structure designing approach with the help of available EDA environment.

II. GROUND BOUNCE

This type of noise comes into existence whenever a high frequency voltage transfers thorough a ground connection wire. This phenomenon occurs mainly because of the e.m.f back towards the transistors. Ground bounce depends on so many factors, like the large capacitance of the test system is directly propositional to the ground bounce noise. Ground bounce becomes worse in the higher speed zone, because this can be summarize with the model [2], Large output current =dV/dt [For higher switching speed]. The one of the most important which affects ground bounce is the drive current and transient current. The transient current usually depends on number of output pins, so to reduce the ground bounce concept we need to reduce the number of output pin at a time.

III. GROUND BOUNCE REDUCTION TECHNIQUES

A. *Sleep transistor approach*

Cutoff transistors from supply voltage or ground using sleep transistor. These types of techniques are also called gated VDD and gated GND. However, the additional sleep transistors increase area and delay. The pull up and pull down network will have floating values and thus will lose state during sleep mode. These floating values significantly impact the wakeup time and energy of the sleep technique due to the requirement to recharge transistors which lost state during sleep.

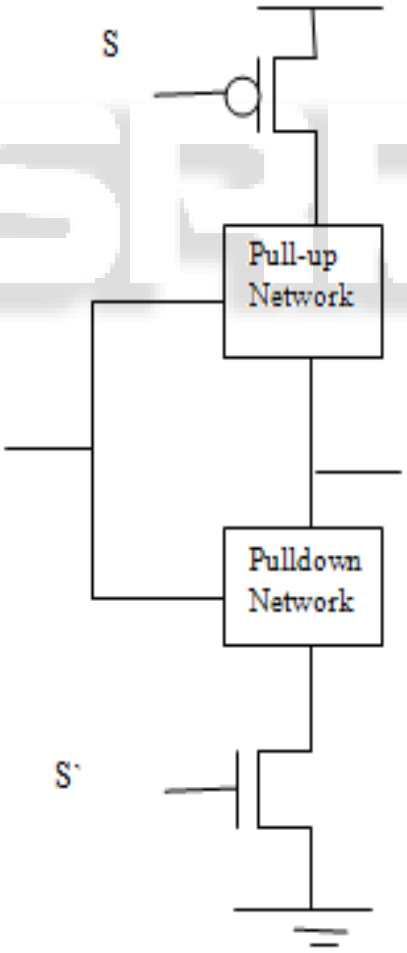

Fig 1: Sleep transistor approach

B. *Power Gating*

Power gating technique for ground bounce reduction is a replica of sleep transistors approach. It uses high threshold

voltage sleep transistors. This method uses low leakage PMOS transistors as header switches. Sometimes the footer switches also used as sleep transistors [1]. The header switches shuts off power supplies to parts of the design in sleep mode and saves power hence reduces the power dissipation.

IV. PROPOSED METHOD

In the proposed method we have used a dual stack of transistor. In this design we have used a chain of four inverters as a base design then applied a power gating structure.

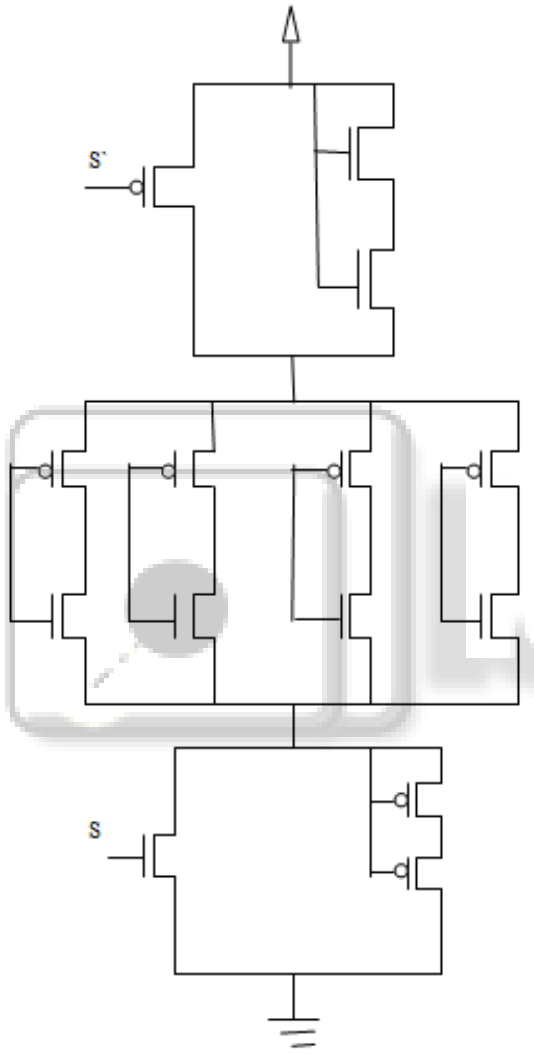

Fig 2: Dual Stack designs for ground bounce reduction

The circuit operation for figure 2 as,

In sleep mode, sleep transistors are off by applying S=0 and S`=1 hence four transistors parallel transistors to these sleep transistors connects with the base design of four inverters with the main power rails. This dual stack approach consists of two NMOS in pull up network and two PMOS in pull down network. The NMOS degrades high logic level while the PMOS degrades the low logic level. This design behaves as pass transistor logic. In this approach if we used a less aspect ratio of transistor nearly about one then it shows a less current flow from these transistors due to the low leakage current. In off mode the set PMOS and NMOS parallel transistors have high threshold voltage. In active mode both sleep transistors and parallel transistors are ON and they works as a transmission gate.

V. SIMULATION

This simulation initially done with base design and then with a power gating structure. This simulation has been done at 90 nm technology.

Base design consists of a chain of four parallel inverters.

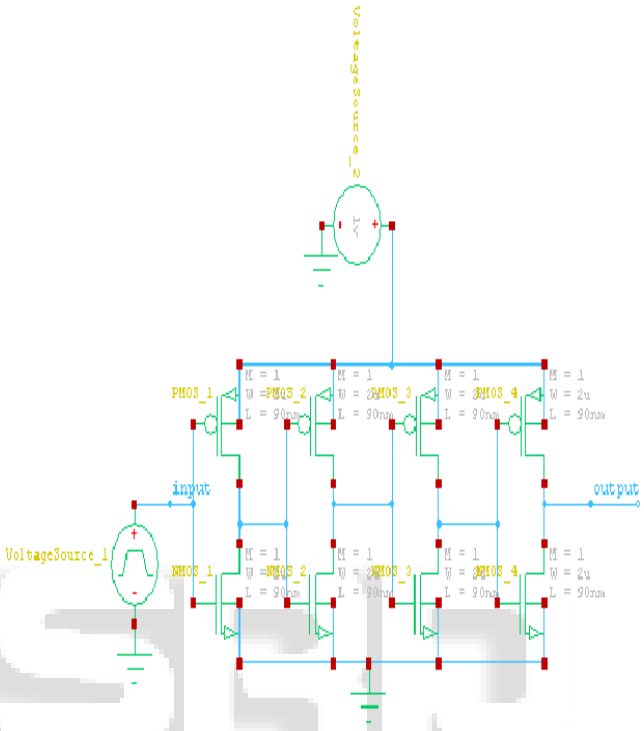

Fig 3: Simulation of base design in 90 nm technology

Power gating structure consist of a chain of four inverters as a main circuit then sleep transistors in pull up and pull down networks, where a chain of 2 NMOS and 2 PMOS in pull up and pull down transistors.

VI. RESULTS

The results of simulative environment show the comparative analysis of previous work on 120 nm technologies to 90 nm technologies. This work uses a 1.0V as a supply voltage, other parameters like power dissipation of base design, power gating structure for both previous works and proposed work has been compared. Some of the results are shown in following table 1.

Properties	Previous work	Proposed Work
Design technology	120 nm	90nm
Supply voltage	1.2 v	1.0v
Power consumption	7.5 µW	~ 0.4 µW(in process)
Reduced Power Consumption	57%	~75 %(in process)

Table. 1: Comparative results of proposed work

VII. CONCLUSION

According to the simulation has done we can see that the power gating is an effective technique to reduce the leakage power consumption of a combinational logic block like a chain of inverter during inactive state. Saving can be as much as 99% of the total power consumption with only proper sleep transistor network. As discussed in the results we still observe some dynamic power consumed in the power gating structure during sleep mode with the change in input due to the possible high leakage current and short current. In this work we have done simulation on 90 nm technology and saves power dissipation near about 75% in comparison with base design.

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