

Analysis of Low Power-High Speed Sense Amplifier in Submicron Technology

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Abstract---In this paper voltage mode sense amplifier, current latch sense amplifier and current sense amplifier is analyzed and simulated with and without MTCMOS technique in a 45nm process technology using Ngspice circuit simulator. When density of memory is increased, the bit line capacitance is also increases and due to that, it limits the speed of voltage sense amplifier. To overcome this problem current sense amplifier is used, which is not dependent on bit line capacitance. This paper shows that delay time is reduced in current sense amplifier compare to voltage mode sense amplifier and current latch sense amplifier but power consumption is increased. MTCMOS technique is used to reduce power dissipation.

Keywords: SRAM, Sense amplifier, Cross coupled Voltage mode sense amplifier, Current latched sense amplifier , Current sense amplifier

I. INTRODUCTION

SRAM is used at where high speed and high performance microprocessor is used. Simultaneously SRAM is also used at where low power is required. When number of SRAM cell is increased to store large number of data, it becomes necessary to use sense amplifier. Sense amplifiers detect the data being read by sensing a small differential voltage swing on the bit-lines rather than waiting for a full rail-to-rail swing. Depending on the performance and power requirements, it's very important for the sense amplifiers to operate fast and do so while burning a minimum amount of power. Conventional Voltage Sense Amplifiers need a minimum amount of differential voltage to be developed on the bit-lines for reliable operation. In digital electronics, the power-delay product is a figure of merit correlated with the energy efficiency of a logic gate or logic family.

II. VOLTAGE MODE SENSE AMPLIFIER

Fig.1 shows the schematic of Cross-coupled voltage mode SA. M1 and M2 are the access transistors, whereas M3-M6 forms cross-coupled inverters. When SAEN is low, M1 and M2 are turned ON and voltage on BL and BLB will be transferred to SL and SLB respectively. Due to positive feedback, higher voltage level goes to VDD and other level goes towards zero.

In the basic cross-coupled SA, the nodes SL and SLB are input and output terminals simultaneously at one time. Hence, the circuit is not being connected directly to the bit line since the circuit would attempt to discharge the bit line capacitance during the decision phase and would increase delay and power [6]. The NMOS devices M3 and M4 in the cross coupled inverter pair as well as the enable device M7 need to be sized for speed since they are in the critical discharge path. Speed is improved if the M7 device is sized higher. But higher widths on M3 and M4 are very important

due to process variations. The initial voltage difference at the output nodes created by bit-line voltage difference may not result in the flipping of the cross-coupled inverters in the right direction if there is sufficient trip point voltage.

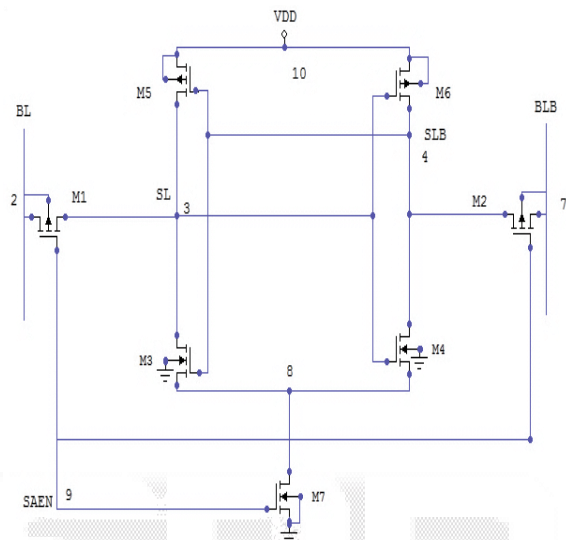


Fig. 1: "Cross-coupled voltage mode SA [10]"

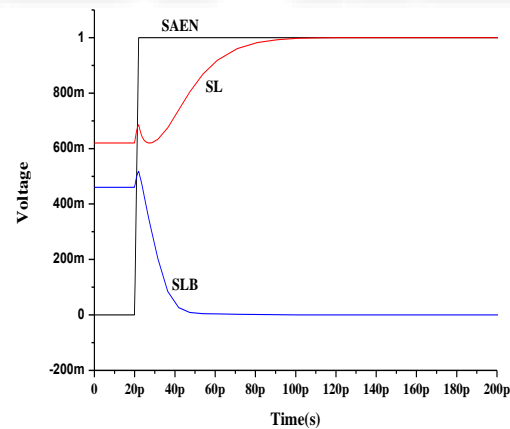


Fig. 2: "Simulation result of cross coupled VSA"

MTCMOS technique can be applied for reducing leakage currents in low voltage circuit in standby mode is based on using two different types of transistor (both NMOS and PMOS) with two different threshold voltages in the circuit. Low V_T transistors are used to design logic gates where switching speed is essential, whereas High V_T transistors are used to effectively isolate logic gates in stand by and to prevent leakage dissipation.

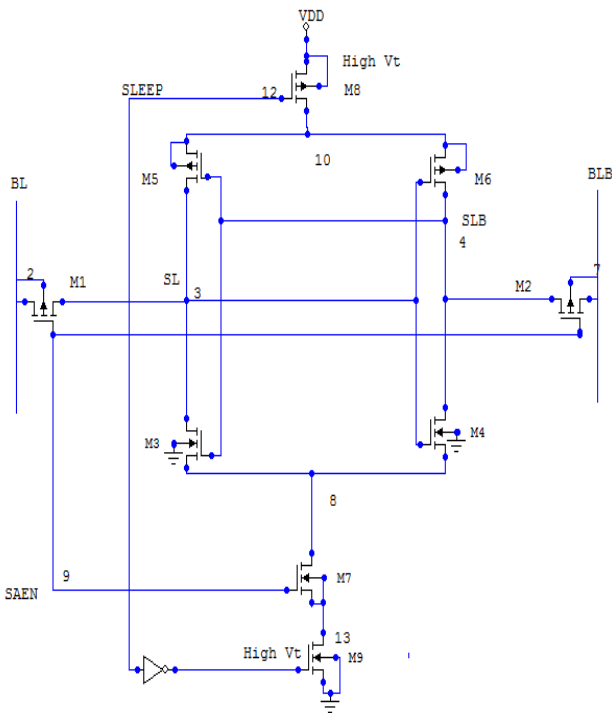


Fig.3: "VSA using MTCMOS Technique"

The working of Voltage mode sense amplifier using MTCMOS circuit is same as Voltage mode sense amplifier circuit but the difference is that M8 and M9 are high V_T MOSFET and rest of MOSFET (M1-M7) are low V_T MOSFET. When SAEN is low, M1 and M2 are turned ON and voltage on BL and BLB will be transferred to SL and SLB respectively. When SAEN is low at that time SLEEP is high so M8 is turned off but due to inverted SLEEP is given to M9, it is also turned off and no leakage current is flow. Hence due to reduction of leakage current, power consumption is also decreased.

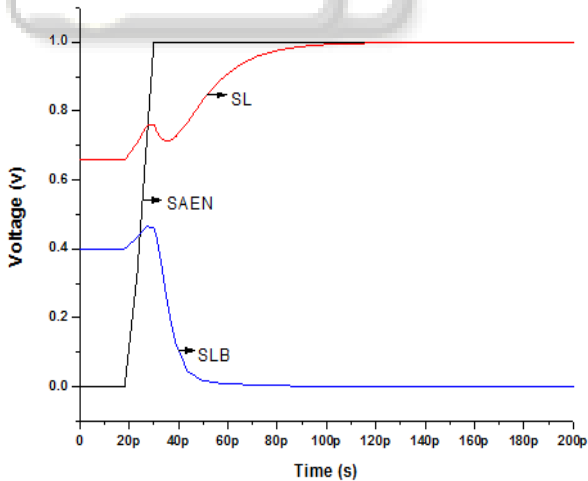


Fig.4: "Simulation result of VSA using MTCMOS Technique"

III. CURRENT LATCH SENSE AMPLIFIER

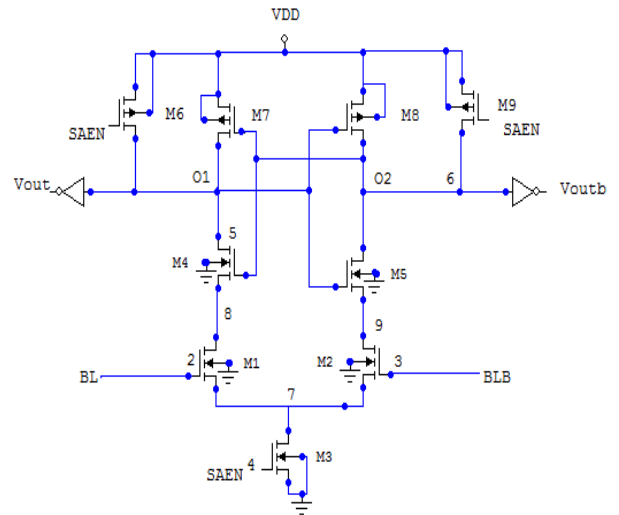


Fig.5: "Current latch sense amplifier" [9].

The current flow of the differential input transistors M1 and M2 controls the serially connected latch circuit. This current latched SA is faster than conventional cross coupled SA. During reset phase when SAEN=0V, the output nodes of the SA (O1 and O2) are reset to VDD through the reset transistors M6 and M9. During evaluation phase when SAEN=VDD, M3 turns ON and the input transistors M1 and M2 starts to discharge O1 and O2 node voltages to GND. Fig. 6 shows simulation results of current latched sense amplifier trying to read data of memory cell containing logic '1'. When word line WL is high to access the memory cell, BLB starts to discharge from VDD and BL remains high. After SAEN is asserted, cross coupled inverters amplify small differential voltage.

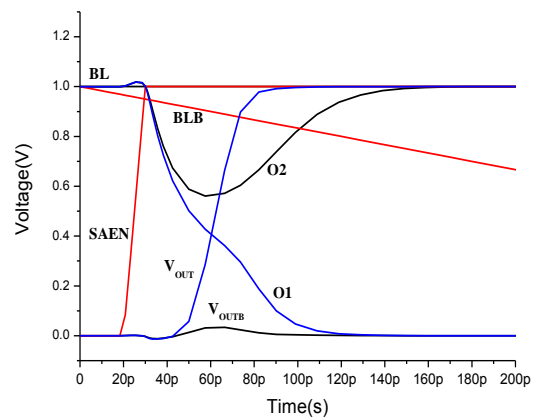


Fig.6: "Simulation result of CLSA"

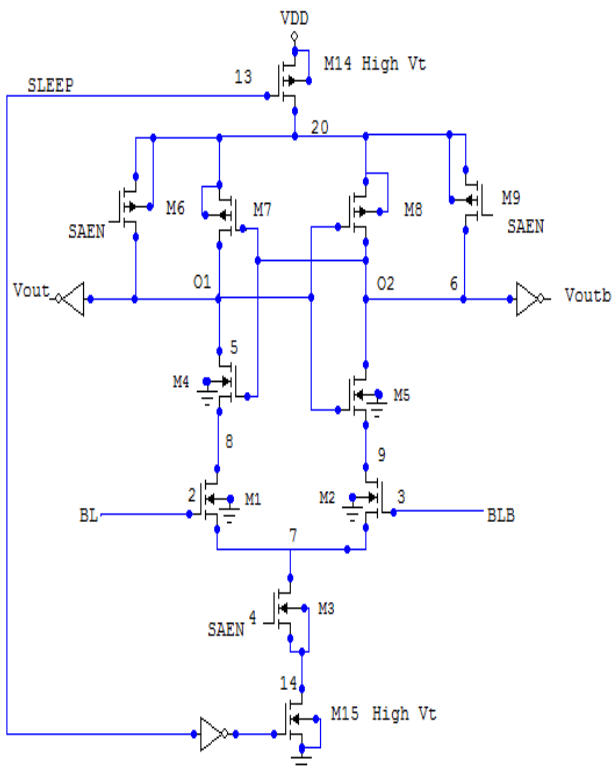


Fig.7: "CLSA using MTCMOS technique"

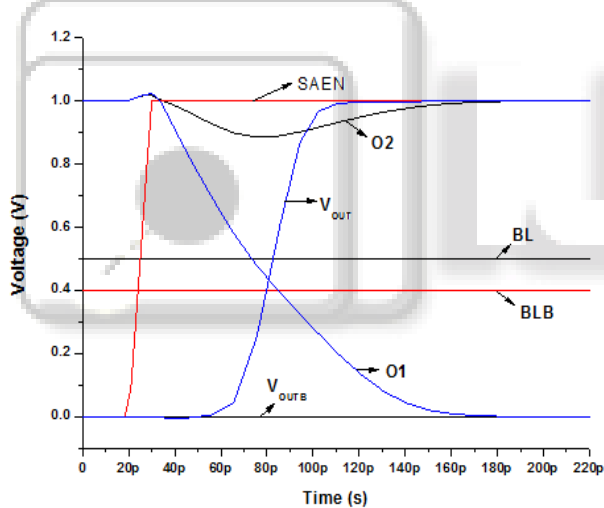


Fig.8: "Simulation result of CLSA using MTCMOS technique"

IV. CURRENT SENSE AMPLIFIER

The current sense amplifier operates in two phases: pre charge and evaluate. During the pre-charge phase, the bit-lines are pre charged through pre charge devices connected to the bit-lines. The Output nodes SA and SA# are also pre charged high through M11 and M12 PMOS devices.

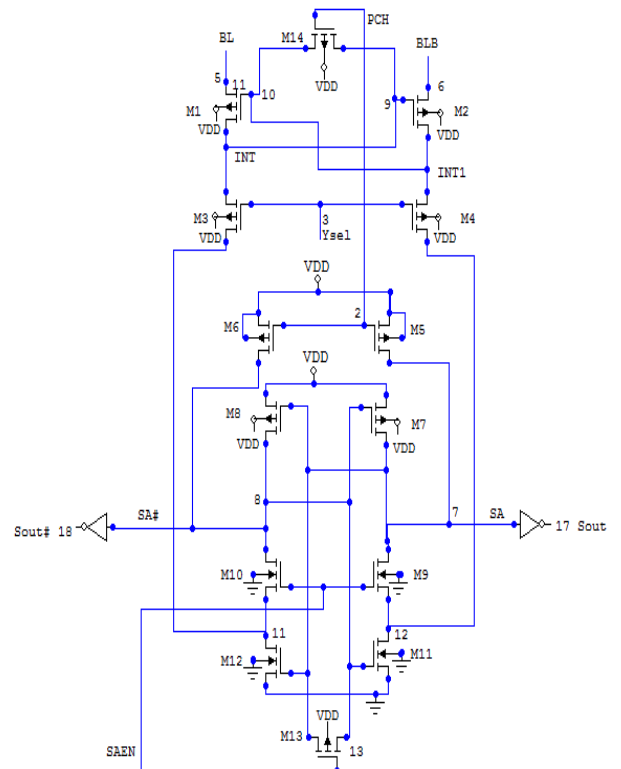


Fig.9: "Current sense amplifier" [8].

The operating current of the sense amplifier is determined by the sizes of devices M5-M8. At the end of the pre charge phase, pre charge and equalization devices M11-M13 are turned OFF. During the evaluation phase, Y_{sel} is pulled low and current is immediately transported to the nodes A and B through the drains of M3 and M4.

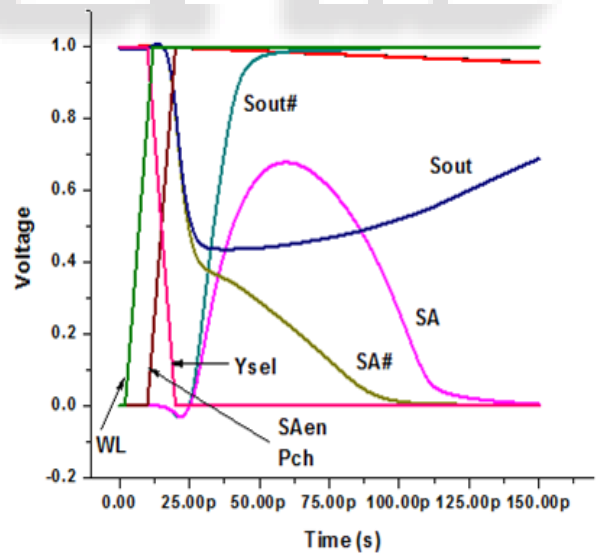


Fig.10: "Simulation result of CSA"

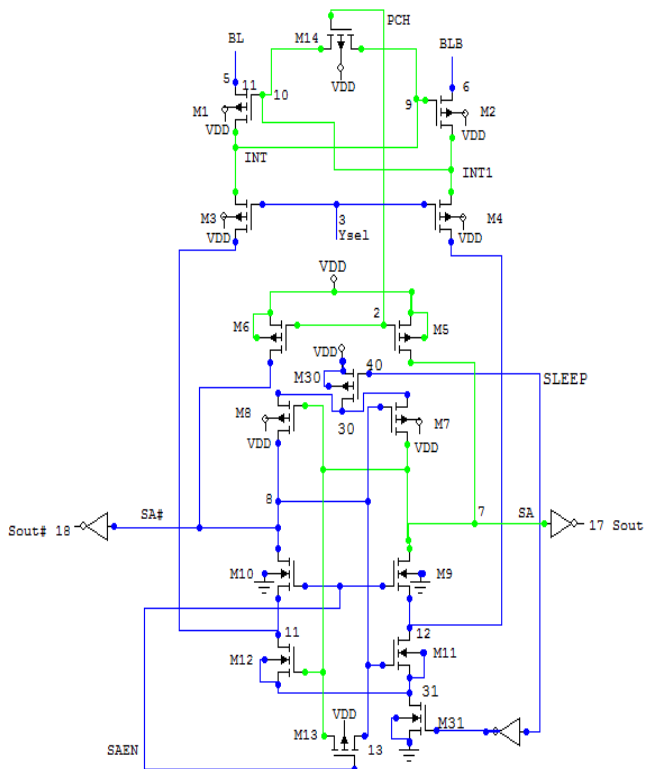


Fig. 11: “Current sense amplifier using MTCMOS technique

The difference in current flowing through A and B will be equal to the cell current. The sense amplifier is enabled two-inverter delay after the SAen is pulled high during which bias current flows through two legs of the sense amplifier, while M14 keeps the output equalized. After this two inverter delay, M14 is disabled and the differential current causes a differential voltage to be developed at SA and SA#. This differential voltage is then amplified to CMOS logic levels by the high-gain positive feedback cross-coupled inverters formed by M5-M8. The sensing delay is relatively insensitive to bit-line capacitance as the operation is not dependent on the development of a differential voltage across the bit-lines. The CSA have low voltage swing on bit-lines. This is because the cross coupled PMOS pair M1 and M2 cuts off the discharge path to ground for both bit-lines. If BL is high and BL# is low.

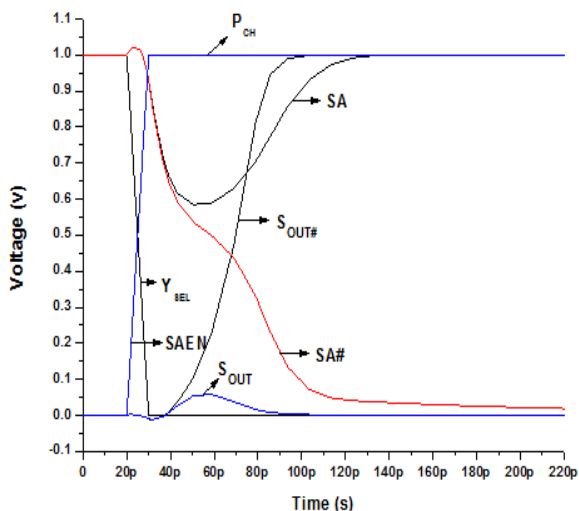


Fig.12:“Simulation result of CSA using MTCMOS technique”

This causes nodes Int and A to go high causing M2 to be cut off. Therefore, the path from the low going BL# to ground is cut off, reducing the voltage swing on it. This scheme enhances the speed of the sense amplifier further due to the fact that there is a flow of bias current before the sense amplifier is actually enabled. Fig.11 shows the Current sense amplifier using MTCMOS technique. In CSA using MTCMOS technique high threshold voltage MOSFET is used so that power dissipation is reduced.

V. PERFORMANCE SUMMARY OF SA

All three types of sense amplifiers are simulated in 45nm technology using NGSPICE. Table 1, shows performance summary of these sense amplifiers.

SENSE AMPLIFIER CIRCUIT	PARAMETER			
	Delay (ps)	Current (μA)	Power Consumption (μW)	PDP (fj)
VSA	52.11	47.33	47.33	2.47
CLSA	49.68	63.98	63.98	3.18
CSA	30.65	362.28	362.28	11.10
VSA using MTCMOS	57.23	28.64	28.64	1.64
CLSA using MTCMOS	55.32	41.43	41.43	2.29
CSA using MTCMOS	45.97	158.05	158.05	7.27

Table1. “Comparison of different types of SA”

VI. CONCLUSION

Cross Coupled VSA, Current latched SA and Current SA is analyzed and simulated in 45nm CMOS technology using Ngspice. From the simulation result, Current Sense amplifier (CSA) is the best choice with minimum delay of 30.65 ps but power consumption 362.28μw which is higher than VSA and CLSA. Power dissipation is reduced by using MTCMOS Technique in VSA, CLSA and CSA. PDP is also decreased by using MTCMOS Technique.

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ACRONYMS

SRAM	Static random access memory
SA	Sense amplifier
VSA	Voltage sense amplifier
CLSA	Current latch sense amplifier
CSA	Current sense amplifier
MTCMOS	Multi threshold Complementary Metal Oxide Semiconductor
PDP	Power delay product

