Modeling and Analysis of Design in MTCMOS Layout in VDSM

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Abstract---For low power design supply voltages and threshold voltages are reduced with advanced 35nm CMOS technology. Lowering the threshold voltage introduces the increase in leakage current. This technique disconnects the low Vth switching block from power supply line and ground line by cutting off high Vth sleep transistors whenever circuit is in idle mode. In this paper, we present a multi threshold CMOS technique to reduce the leakage current as well as it controls the ground bounce noise. This was done by using changing of CMOS design to tri-state MTCMOS transistor. In an MTCMOS circuit, high threshold voltage (high-|Vth|) sleep transistors (header and/or footer) are used to cut off the power supply and/or the ground connections to an idle low threshold voltage (low-|Vth|) circuit block. The propagation delay and the dynamic switching power consumption of active logic blocks can be thereby increased. Multiple autonomous power and ground gated circuit domains are typically utilized for effective control of leakage power consumption in MTCMOS circuits. This is enhanced version of MTCMOS technique to suppress the ground bounce noise. A further high Vth PMOS called Dozer is connected in parallel with footer sleep transistor. The new model, verified by TANNER simulations and measured data, includes delay, area and low power consumption result shows the better performance rate of this proposed system and also make that in 32nm size with that application of Switched Bank circuit.

Keywords: MTCMOS, Switched Bank circuit, CMOS buffer, 32nm, VDSM, Delay, Power consumption, Area.

I. INTRODUCTION

Very-large-scale integration (VLSI) is that the method of making integrated circuits by combining thousands of transistors into one chip. VLSI began within the Seventies once advanced semiconductor and communication technologies were being developed. The microchip could be a VLSI device. VLSI became associate degree early trafficker of normal cell (cell-based technology) to the merchandiser market within the early 80s wherever the opposite ASIC-focused company, LSI Logic, was a frontrunner in gate arrays. VLSI‟s cell-based giving, the technology had been primarily accessible [2] solely inside massive vertically integrated corporations with semiconductor units like AT&T and IBM. Complementary metal–oxide– semiconductor (CMOS) could be a technology for constructing integrated circuits. CMOS technology is employed in microprocessors, microcontrollers, static RAM, and different digital logic circuits. CMOS technology is additionally used for many analog circuits [3] like image sensors (CMOS sensor), knowledge converters, and extremely integrated transceivers for several styles of communication. Frank Wan lass proprietary CMOS in 1963.CMOS is usually brought up as complementary- symmetry metal–oxide–semiconductor (or COS-MOS). The complementary- symmetry seek advice from the very fact that the everyday digital style vogue with CMOS uses complementary and symmetrical pairs of p-type and n-type Metal compound Semiconductor Field impact Transistors (MOSFETs) for logic functions. Consequently, CMOS devices don't turn out the maximum amount waste heat as different kinds of logic, as an example Transistor–Transistor Logic (TTL) or NMOS logic, that commonly have some standing current even once not dynamical state. CMOS additionally permits a high density of logic functions on a chip. It had been primarily for this reason that CMOS became the foremost used technology to be enforced in VLSI chips. Styles for a non-inverting CMOS buffer that drives a given load at 1GHz. the full circuit should [1] maintain noise margins higher than .5V, and should work inside an outlined space. Most CMOS gates, inverters and high-current IC merchandise were unbuffered and exhibited smart logic-system performance, speed, noise immunity and quasi-linear characteristics in an exceedingly wide range of applications. Whereas initial buffered merchandise were confined to OR and AND functions, buffered NOR and NAND gates were introduced with constant generic 4000A-series designations because the original wide used unbuffered gates. Users were stunned by the non-interchangeability of the devices in applications wherever speed, noise immunity, output resistance, and linear gain-bandwidth characteristics were crucial. Its profit to CMOS users to possess accessible the definitions and designations of each [14] buffered and unbuffered. B-series CMOS devices as determined by the JEDEC CMOS Standardizing Committee underneath the cognizance of the JC40.2 JEDEC Committee of EIA. Comparisons of user-oriented characteristics and therefore the use of buffered and unbuffered gates are reviewed. A buffered CMOS device is one that the output ON resistance is freelance of any and every one valid input logic conditions, each preceding and gift is alleged to possess a buffered output or to be a buffered CMOS device. Which in proposed in 32nm and place in a Switched Bank circuit with the voltage at zero level.

II. EXISTING METHOD

The existing system, take into account Associate in Nursing overshooting result in nanoscale model, by together with the sub threshold region wherever the overshooting result seems. The most contribution is to review the result of overshooting result once applying 65nm technology to the model conferred. However it's noticed that the authors failed to take into account [9] the overshooting result that could be a vital physical facet and seems in nanometer regime of CMOS gate analysis. Associate in nursing analytical expression for nanoscale CMOS inverters is targeted during this system. Taking into thought the aspects

that ought to be thought of, so the models in nanoscale maintain accuracy and to reduce the error share compared to plain simulators. Additionally to it, simplicity ought to be thought of to avoid heavy-weight computations. This content of the overshooting result caused a better error once smaller technologies square measure applied. If the overshooting, result that modifies the model by modeling this result as (Huang et al 2010) done to the model, that could be a vital from (Rosello and Segura 2011) in modeling submicron CMOS submicron gates.

III. PROPOSED WORK

This system projected a thought of forty five nm CMOS buffer arrangements is enforced and additionally to scale back the delay rate of buffer output in low input power vary. Simulation output provides reduced delay performance in 45nm which supplies less time delay than existing sized CMOS. CMOS buffer within the variety of PI section electrical device and electrical condenser style based mostly projected CMOS equivalent circuit is enforced. Considering in account of delay, power consumption and space mistreatment 32nm technologies to implement the new variety of shift CMOS corresponding to style. For wide conductors with W & H, capacitance to substrate (of any ground plane) determined as a parallel plate electrical condenser C = εA/t wherever A is that the flattened space of the wire and t is that the thickness of the compound for many real conductors in these days. IC technology, fringing fields contribute a significant a part of the road capacitance and should be enclosed within the capacitance calculations. For W, W≈H, fringing fields add quite the parallel plate portion to the overall line capacitance. The Model of Switched bank circuit is implemented on the layout which the ground is perfectly neutralised.

IV. ANALYTICAL OF BUFFER MODELING

VLSI circuit analysis within the circuit level for the foremost vital measurements, like delay and power consumption depends on rigorous modeling of their basic parts [9]. One in every of the foremost prevailing and underlying parts in digital systems is that the CMOS buffer in Fig 1. A buffer may be a straightforward however principal and important part has several significant applications and it immensely used for signal clean up and therefore the reduction of delay, noise and interference. This buffer is well-liked due to its low power consumption chiefly in shift phases. Hence, several researchers have self-addressed this want by proposing numerous analytical models to gift the behaviour of CMOS buffers.

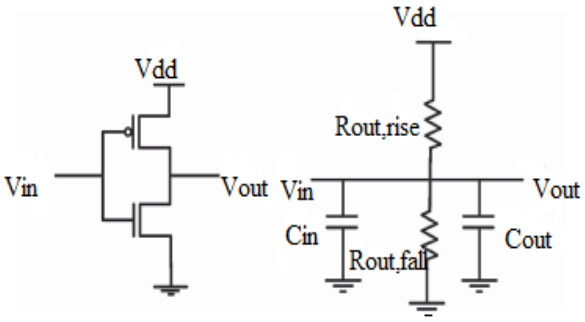


Fig.1: CMOS Buffer

V. ALPHA POWER MODELING

The Alpha-Power Law MOSFET Model is that the most generally used compact drain current model because of its straightforward mathematical kind and high degree of accuracy [8]. The model doesn't describe the sub threshold region and thus on/off drain current trade-offs can't be totally analysed. The Low Power transregional MOSFET model describes all regions of operation (sub threshold, triode, and saturation). Therefore, the Low Power Trans regional Model is associate degree advantageous selection for predicting performance of future technology generations and above all for analysing on/off drain current trade-offs [6]. Coupling the Alpha-Power Law and Low Power Trans regional models permits a replacement compact physics primarily based Alpha-Power Law MOSFET Model. The three region model assumes that the output current may be a linear performs of the input voltage. This can be truly solely the case for a totally speed saturated device. For a tool with no speed saturation this may be a perform of the sq. of the input voltage [12]. Most up-to-date devices have fall time, somewhere in between these two extremes. This can be taken into consideration by introducing a brand new curve fitting parameter α and writing the output current as follows:

$$\text{Iout (t)} = \min\left(\frac{(V_{in}(t)-V_T)\alpha W}{R_M}.\frac{V_{out}(t)W}{R_F}\right) 1\le\alpha\le 2 \quad (1.1)$$

In this approach utilized by Nabavi-Lishi is termed the alpha-power law model. A similar input wave kind is assumed for the three region model Vout (t) Power consumption, space and delay area unit resolved within the same means [12]. The employment of α within the expression for current is that the solely initial assumption that is completely different from the three region model. For the case wherever α= one the alpha-power law model is a dead ringer for the three region model. Once approximating delays to VDD=2 (ΔVout = zero.5) the result most frequently falls within the linear region. Therefore, the easy approximation the opposite two regions area unit unnoticed and also the linear region equation is employed alone.

$$I_D \approx \frac{T_{in}(\alpha+V_T)}{1+\alpha}+\frac{T_M\Delta V_{out}}{1-V_T} \quad (1.2)$$

This single equation and the three region estimate given in equation are simply the sum of two stipulations. One proportional to the input slew time and one relative to the capacitive load. For any value of α only differentiation between these equations values of VT and RM used to fit a given set of information. Therefore, when using this single equation approximation the alpha-power law model and the three region model are identical [9].

VI. 32 NANO METER TECHNOLOGY

A low-power 32 nm technology could be a continuation of the joint development initiative between Samsung manufactory and JDA alliance partners [5]. Various products from high fables players are in production since 2008 enabled by 32nm low power method technology and its style scheme. The 32nm method is characterized by many key technologies, that offers 193nm immersion lithography patterning of important style rules with radial asymmetry rates cherish dry litho systems. Also, suggests

immoderate Low-K non-conductor materials for metal line insulation leading to RC delay reduction vs. low-k. Increasingly, for semiconductor makers moving to advanced nodes – 90nm, 65, 45and below the best challenge is lithography. This is often as a result of lithography is essentially affected by basic principles of optical physics. At 65 nm, a line is a smaller amount than a third of the effective wavelength because the business moves forward; optical phenomenon and interference have become elementary obstacles, not simply second order effects [15]. Inverse Lithography Technology (ILT) has been explored for several years. Though these early approaches to ILT usually resulted in very good lithography, they're usually impractical in an exceedingly production setting. Runtimes area unit several order of magnitude too slow, and therefore the ensuing masks area unit usually too complicated to manufacture.

A. *Cmos Layout*

High-performance VLSI design is attracting much attention because of emerging need for miniaturization, and hence design optimization for trading-off power and performance in nanometer scale integrated circuits is the need of the present scenario, which demands a decrease in both supply voltage VDD (to maintain low power dissipation) and threshold voltage Vth (to sustain propagation delay reduction), but the fact is that the decrease in Vth not only increases leakage power but also short circuit power. While operational in Nano scale technology the total power dissipation of clock drivers, which generally have CMOS inverters, are quite large and have 30 to 50% share only of leakage current and short circuit current Reduction of power dissipation in CMOS digital circuits has become an ever more important design optimization goal. Although there are several bases of power dissipation in the CMOS technology, most of the existing power optimization and estimation techniques have focused on the dynamic power dissipation due to the charging and discharging the load capacitances at the gate outputs.

The other major source is the short circuit power dissipation which is due to the simultaneous conduction of the PMOS and NMOS transistors during the input transitions. For example, for high performance circuits, if large gates are used to drive relatively small loads and if the input transition time is long, then P becomes quite significant.

In 32nm layout with the model arrange in the field, PMOS and NMOS combining in CMOS is with the layout form model can be implement on the basic form with the alpha power law model.

Here the layouts have the low power function of the 32nm design, channel carrier moves much faster.

We used the given typical parameters of the CMOS, so the only variable that we really needed to adjust was the aspect ratios (W/L) of both the NMOS and PMOS devices, and the positive and negative power bars.

During this temporary, we've supposed a pure electrical phenomenon load, for NMOS and PMOS transistors of the buffer. At the start of the rising input, the PMOS semiconductor unit is within the sub threshold region. The result of this current is heavy in VDSM CMOS technologies

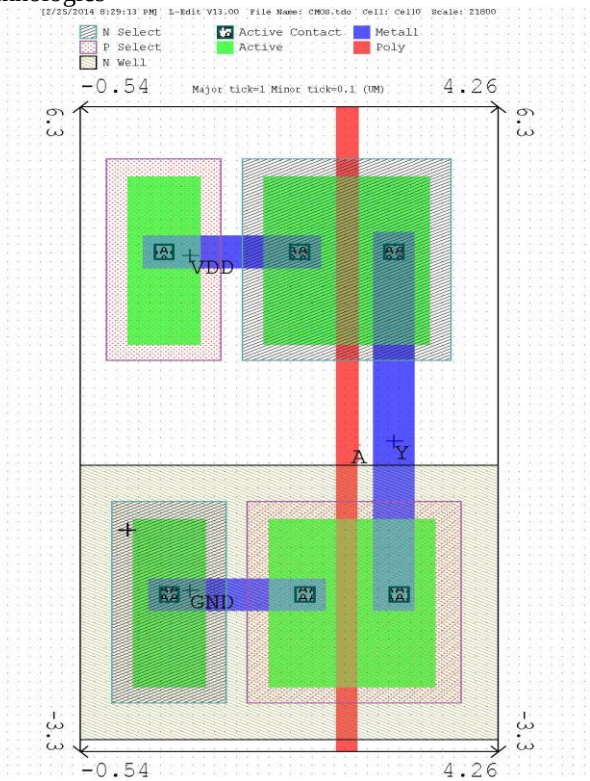


Fig.2: CMOS Buffer layout in 32nm

PMOS version of input buffer can be used for lower input signal levels but has a larger offset. To avoid the offset, the NMOS buffer can be used in parallel with a PMOS buffer

B. *Switched Bank Circuit (SBC)*

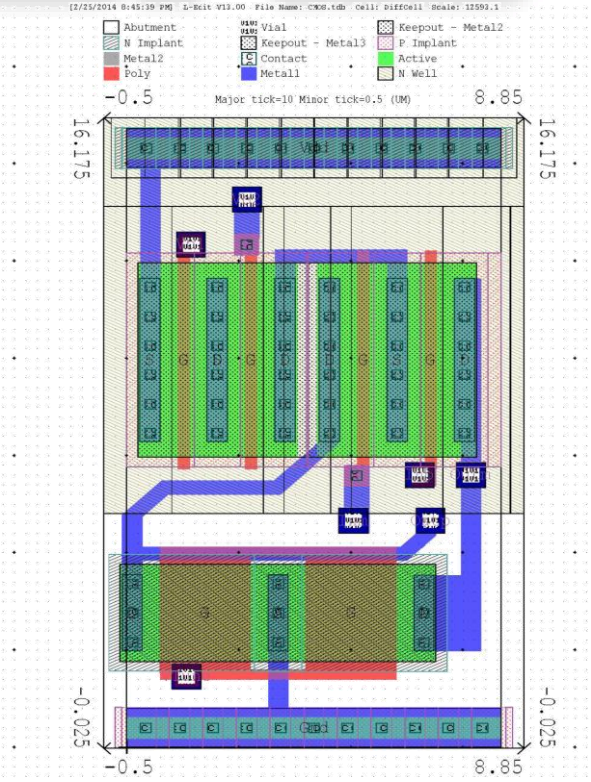


Fig.3: Switched Bank circuit in 32nm

An easy way to neutralize the ground voltage in the layout of a circuit we use the switched bank circuit. Here the model is more efficient than the previous model.

VII. Result And Analysis

In VDSM, the semiconductor unit model isn't any longer valid. This happens as a result of short channel effects like quality degradation, drain elicited barrier lowering, and speed saturation [9]. Therefore, so as to accomplish a much better analysis, a lot of correct model is needed.

Time delay for 2 CMOS
Buffer in series = absolute (time taken for i/p signal
- Time taken for o/p signal
= abs (18-34) psec
= 16 psec
For single buffer = 8 psec

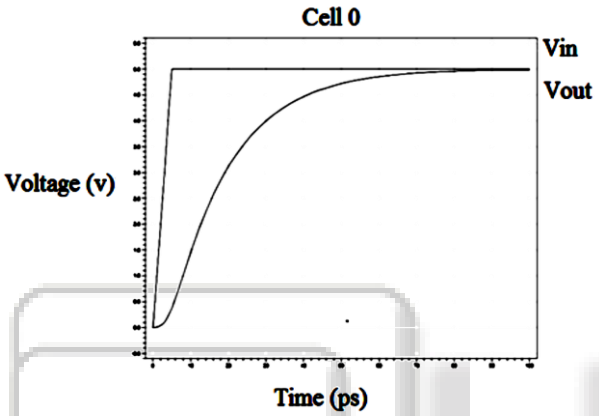


Fig.4: Delay waveform

The area size comparison is given in following Table 1

Tech Node (nm)	Physical Gate (nm)	Tox (nm)	K	V_{th} (V)	Na/ (cm^3)	Nd/ (cm^3)
130	90	3.0	3.7	0.34	1.0e16	1.0e19
90	53	2.4	3.0	0.32	1.4e16	1.4e19
65	32	1.7	2.5	0.29	2.0e16	2.0e19
45	22	1.5	2.0	0.29	2.9e16	2.9e19
32	12	1.2	1.7	0.28	3.0e16	3.0e19

Table. 1: Comparison of area size

The comparison of delay and power consumption is given in following table 2,

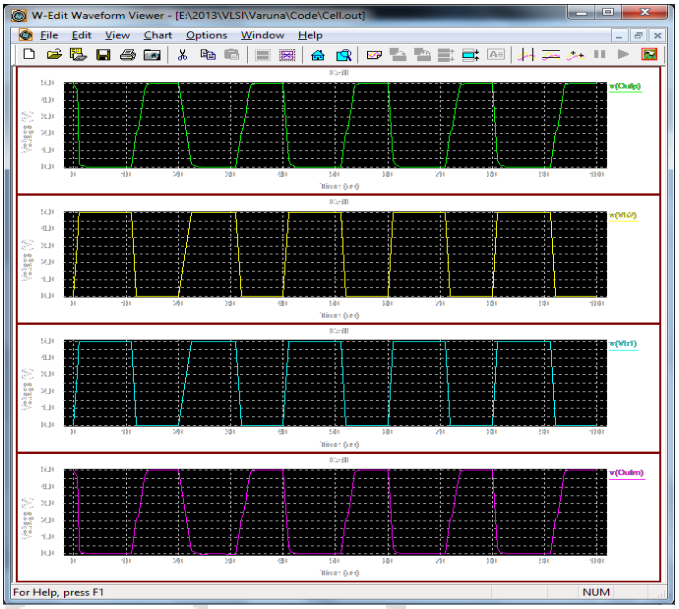
	130 NM	90 NM	65 NM	45 NM	32 NM
DELAY	15.4 Psec	13.3 psec	11.2 psec	9.5 psec	8 psec
POWER	6.124 mW	5.186 mW	2.277 mW	0.692 mW	0.541 mW
VOLTAGE	1.2v	1.1v	0.9v	0.8v	0.5v

Table. 2 : Comparison of delay and voltage

A traditional CMOS buffer is created of NMOS and PMOS transistors, as delineate. For temporal arrangement analysis, of these model parts should be averaged in time once the signal passages between two low and high values. The particular in operation regions (linear or saturation) within the quantity trust on the kind of load driven by the buffer. During this temporary, we've supposed a pure electrical phenomenon load, for NMOS and PMOS transistors of the buffer. At the start of the rising input, the PMOS semiconductor unit is within the sub threshold region. The result of this current is in VDSM CMOS technologies.

Using BDSM technology to scale back the world, delay and power consumption for CMOS buffer improve to 32nm technology. With the scaling of CMOS technology into the terribly deep sub micrometer (VDSM), buffer modeling has been an essential demand.

VIII. Output Waveform



IX. Conclusion

New threshold voltage tuning techniques for Tri-mode MTCMOS are used to reduce the ground bounce noise and sub-threshold escape current. The ground bounce noise is reduced in the mode transition. Tri –transistor is the best technique to reduce the leakage current. Leakage current has been decreased with the increase in size of the transistor. We have presented a power-up sequence generation method to address the problem of minimizing ramp-up time under peak inrush current constraint for tri-state designs. The proposed framework includes a current budget algorithm based on an effective model, an analytical routing guidance and a configurable domino-delay controller. We have to extend our work to analyze the impact of decoupling capacitance on ramp-up time, inrush current and dynamic IR drop. Considering the inductance imposed by the package would result in a different inrush current estimation.

Here the method of using the model we can implement the 32nm CMOS Buffer model and also the Switched Bank Circuits with efficient range of power and delay in the circuit

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