Analysis and Closed Loop Control of Soft Switching High Gain Converter with Coupled Inductor

Erupaka Maheshreddy[1] Dr. Swapnajit Pattnaik[2]
[1]M.Tech. Student [2]Assistant Professor
[1, 2]Department of Electrical & Electronics Engineering
[1, 2] VNIT Nagpur, India.

Abstract—In this paper a soft switching high gain dc-dc converter is analyzed and its closed loop control is done using voltage mode PI controller. The Converter will be having less input Current ripples due to its interleaved structure which is quite useful for renewable applications. Due to soft switching of the converter it will be having less losses and more efficiency. The converter uses coupled inductor which will have turns ratio less than unity for getting desired gain. By obtaining closed loop operation of the converter the efficiency of the converter is further improved and the optimal usage of the converter with variable source (renewable) and load conditions. The closed loop operation of the converter is simulated for 600w prototype using PSIM 9.0 and its waveforms are presented at different operating conditions.

Key words*:* Coupled Inductor, Soft Switching, Voltage control, Renewable energy.

I. INTRODUCTION

Renewable energy sources are one of the significant players in the world's energy portfolio. Generally they deliver DC power at low voltage with higher current. Therefore, a suitable power electronic interface is required for standalone/grid connected applications. The output voltage generated by the photovoltaic arrays, the fuel stacks, the super capacitors or the battery sources is relatively low, even lower than 48V. It should be boosted to a high voltage, such as 380V for the full bridge inverter or 760V for the half bridge inverter in the 220V AC grid-connected power system as shown in Fig. 1.

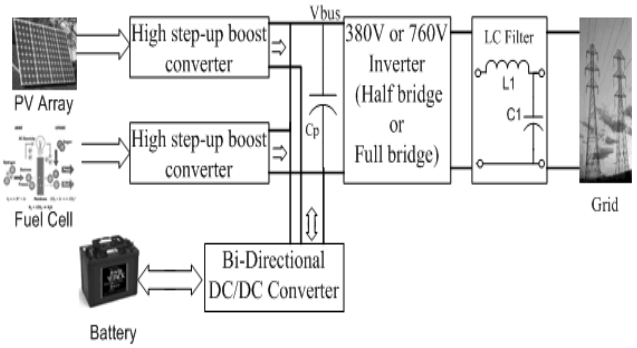


Fig. 1: Single-phase hybrid renewable energy grid connected system

How to realize high step- up DC/DC converters with high performance is one of the main issues in the renewable energy applications.

The Closed loop operation of the Dc-Dc Converter is necessary for maintaining constant dc link voltage to the Inverter and for supplying power to varying load conditions.

A. *Limitations of Conventional Boost Converter*

1) The *1/ (1-D)* characteristic require large duty cycles for large voltage boosts. Large duty cycles are a problem at high frequencies when the switch may not have sufficient time to turn off before the start of the next switching period.
2) Parasitic effect such as inductor DC resistances limits gain at large duty cycles and result in low converter efficiencies. The dissipated energy causes heating and requires additional thermal management

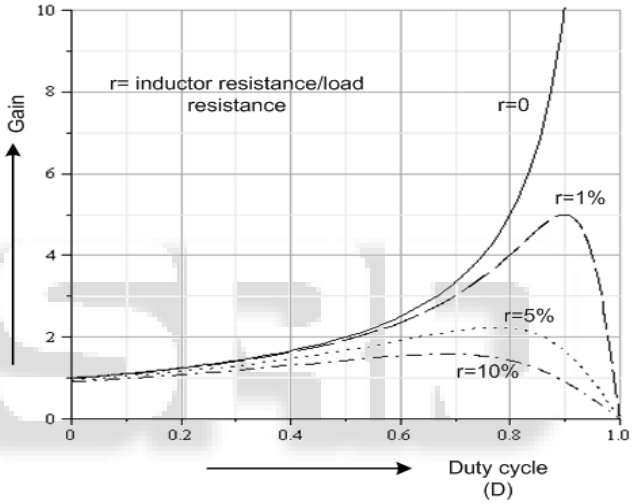


Fig. 2: Boost gain (CCM) vs. duty cycle *D*

Fig. 2 shows the voltage gain of the conventional continuous conduction mode(CCM) boost converter plotted vs. *D* for several values of inductor DC resistance *r* (expressed as a percentage of load resistance). For practical values of *r* in the low power range (between1% and 5%) the maximum gain is limited to less than 5 V/V.

II. DESCRIPTION OF PROPOSED CONVERTER

In this Converter, winding coupled inductor is used as both forward and fly back converter. This thus allows the use of switched capacitor technique by charging the capacitor when the coupled inductor behaves like forward converter and discharge in series when the coupled inductor behaves like forward converter and discharge in series with the converter. Active clamping technique is used to achieve zero voltage switching (ZVS) turn on of main switches. The leakage inductance of coupled inductor controls the diode turn off current falling rate, turning them off by zero current switching (ZCS) and alleviating the reverse recovery problem. Hence the switching losses are reduced which adds to reduced cost and smaller size of converter. The Converter have interleaved converter modules which reduces the input current ripple significantly operated with interleaved PWM

technique, i.e. gating pulses is shifted by half of switching time period (T).

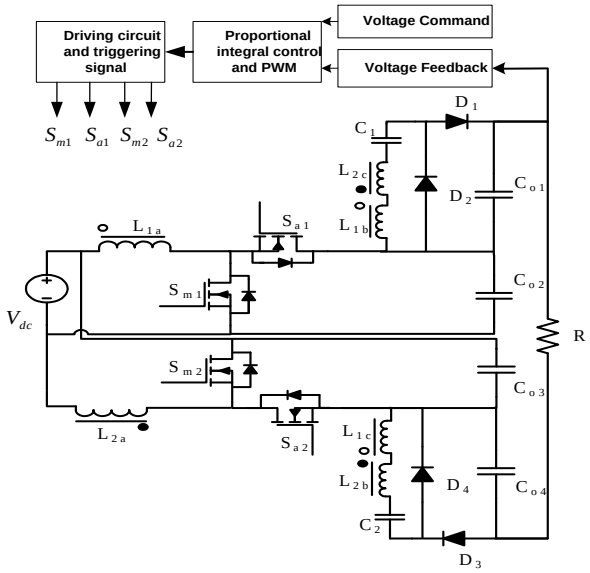


Fig. 3: System Configuration of proposed converter

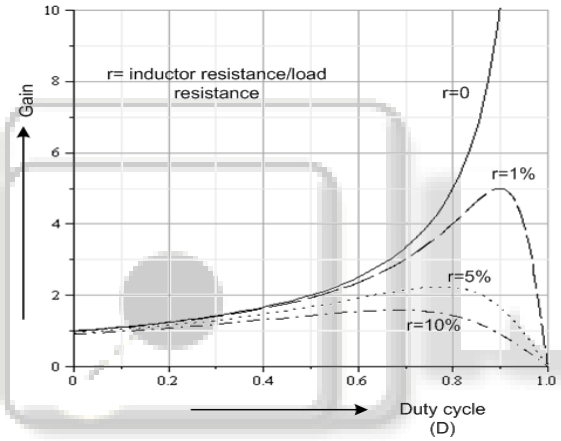


Fig. 4: Normalized input current ripple versus the duty cycle and interleaved phases

A. Analysis of the Converter

The converter operates in 20 modes. Due to symmetry of the circuit only first 10 modes are analyzed here.

Mode1. (t0-t1):]: In this mode, the main switches S_{m1}, S_{m2} are closed and the auxiliary switches S_{a1} and S_{a2} are off. Diodes D_1, D_2, D_3 and D_4 are reverse biased, hence no current flows through secondary winding. Magnetizing and leakage inductor are charged linearly by the DC input source V_{in}.

$$i_{Lm1}(t) = \frac{V_{in}}{L_{m1} + L_{lk1}} t + I_{Lm1}(t0)$$

$$i_{Lm2}(t) = \frac{V_{in}}{L_{m2} + L_{lk2}} t + I_{Lm2}(t0) + I_o$$

Mode 2. [t1 – t2]: In Fig. 3 at t1, main switch S_{m2} is turned off. Since the value of C_{s2} is very small it is charged linearly by magnetizing current which is also equal to current through the leakage inductor. In this mode, V_{cs2} is less than V_{co3} and anti-parallel diode of S_{a2} is off. Due to the presence of parallel capacitor C_{s2}, the main switch S_{m2} is turned off using ZVS condition. The capacitor voltage is expressed as

$$V_{cs2} = \frac{\left[I_{Lm2}(t1) + I_o\right]}{C_{s2}} (t - t1)$$

Mode 3. [t2- t3]: At t2, C_{s2} is charged to V_{co3}, since C_{s2} is smaller all the magnetizing current is diverted to C_{o3} resulting in anti-parallel diode of S_{a2} to start conduct; consequently the voltage appearing across the magnetizing inductance V_{Lm2} decreases as V_{co3} increases according to voltage divider action

$$V_{Lm2} = \frac{L_{m2}}{L_{m2} + L_{lk2}} (V_{in} - V_{co3})$$

The switch S_{a2} should be turned on before i_{lk2} becomes negative for ZVS turn on.

Mode 4. [t3 – t4]: At t3, the magnetizing voltage V_{Lm2} is sufficient to induce coupled inductor secondary voltage to forward bias D_1. Diode D_4 is still reverse biased. Current through leakage inductor i_{lk} is a summation of the magnetizing current i_{Lm} and reflected current i_{D1} through output diode D_1.

$$I_{lk1}(t) = i_{Lm1}(t) + N * i_{D1}(t)$$

$$I_{lk2}(t) = i_{Lm2}(t) - N * i_{D1}(t) + I_o$$

Mode 5. [t4 – t5]: At t4, the auxiliary switch S_{a2} is turned on using ZVS condition because its anti-parallel diode is on. Current paths are same as that of previous mode except S_{a2} is conducting instead of its body diode.

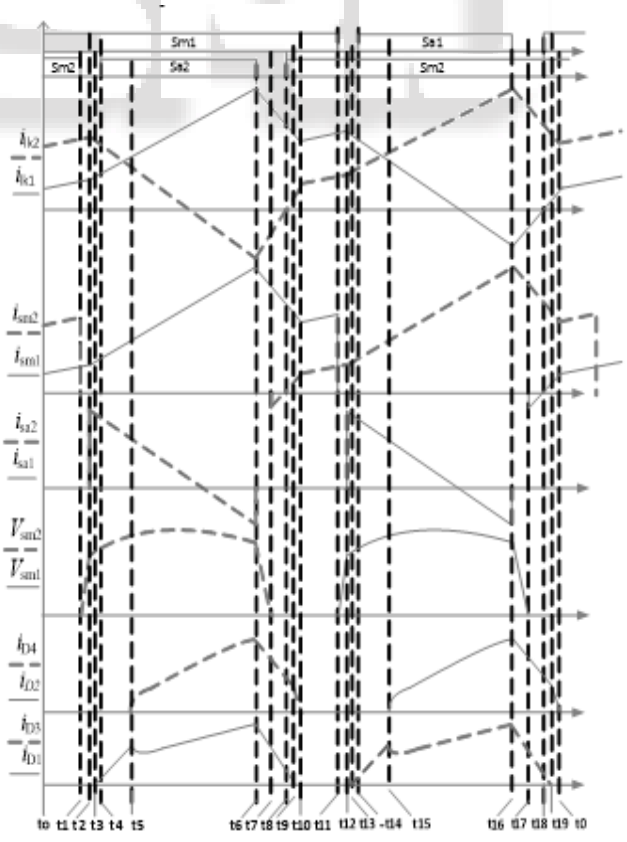


Fig. 5: Operating waveforms of the converter

Mode 6. [t5 – t6]: At t5, the V_{Lm2} is decreased to the value sufficient to forward bias D_4. As the rate of change

of secondary current is controlled by leakage inductance and the voltage across it which is almost constant, the rate at which diode current i_{D1} was increasing in earlier mode is divided between i_{D1} and i_{D4} equally in this mode.

Mode 7. [t6 – t7]: Auxiliary switch S_{a2} is turned off at t6 terminating resonant circuit between i_{lk2} and C_{o3}, and switch capacitance C_{s2} starts discharging in a resonant manner due to the leakage inductance L_{lk2}. The auxiliary switch is turned off using ZVS condition due to C_{s2}.

Mode 8. [t7 – t8]: At t7, capacitor C_{s2} is discharged completely and anti-parallel diode of S_{m2} prevent C_{s2} voltage from going negative. In this interval S_{m2} can be turned on using ZVS condition.

Mode 9. [t8 – t9]: S_{m2} is on, and the transformer secondary current decreases as leakage inductor current i_{lk} increases. At t9 the current through diode D_1 decreases to zero while D_4 is still conducting. The falling rate of diode current is controlled by the leakage inductance and the voltage across it which can be expressed as

$$\frac{di_{D1}(t)}{dt} + \frac{di_{D4}(t)}{dt} \approx \frac{V_{co3}}{2N * L_{lk}}$$

From (8) it is observed that, as the secondary current is divided between two diodes, a small value of leakage inductance is sufficient to achieve ZCS turn off of diodes.

Mode 10. [t9 – t10]: At t9, the transformer secondary current is flowing through D_4 which is decreasing linearly and almost at twice rate as compared to previous mode. At t10, secondary current decreases to zero and D_4 is reverse biased, and the current through L_{lk2} is equal to current through L_{m2}.

$$\frac{di_{D4}(t)}{dt} \approx \frac{V_{co3}}{2N * L_{lk}}$$

A similar operation is repeated in the remaining ten stages of a switching period. Hence the input current ripple has a frequency twice that of the operating frequency. Fig. 4 shows the equivalent circuit of each operating mode in the half cycle of switching period.

Modes(1-10):

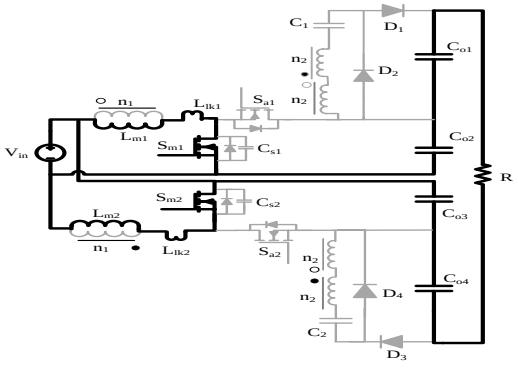


Fig. 6: Mode 1

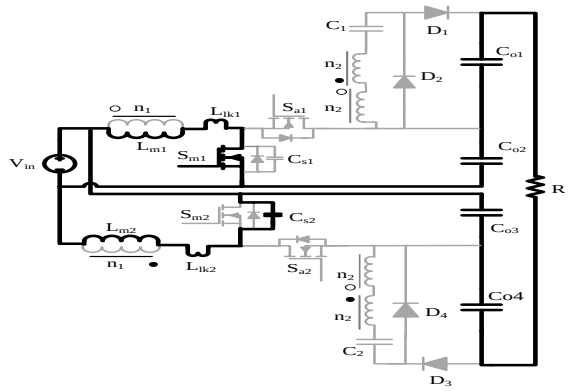


Fig. 7: Mode 2

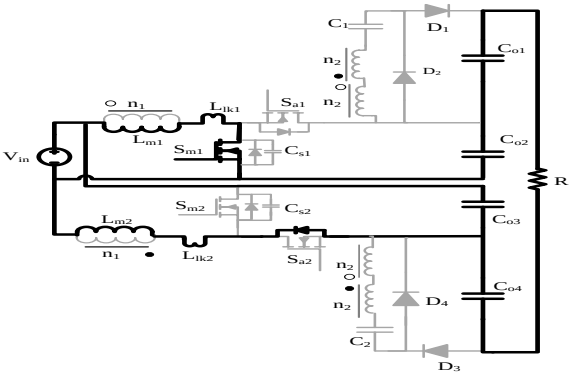


Fig. 8: Mode 3

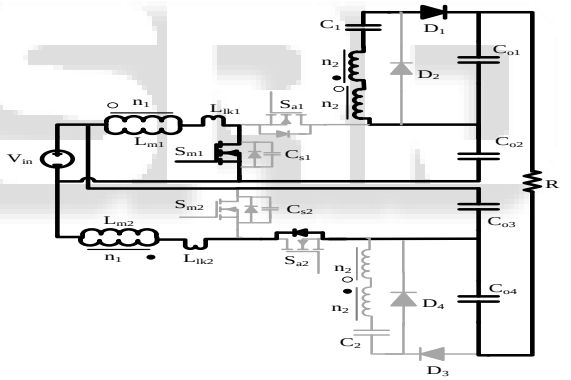


Fig. 9: Mode 4

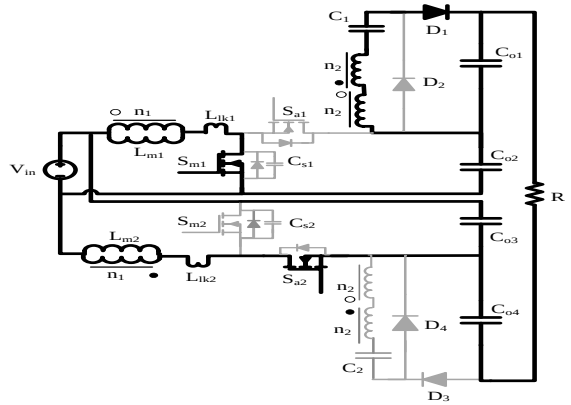


Fig. 10: Mode 5

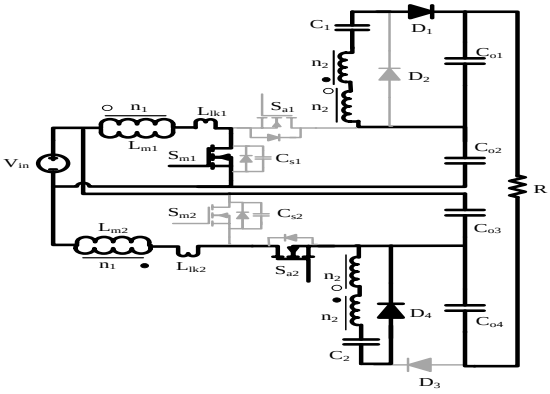


Fig. 11: Mode 6

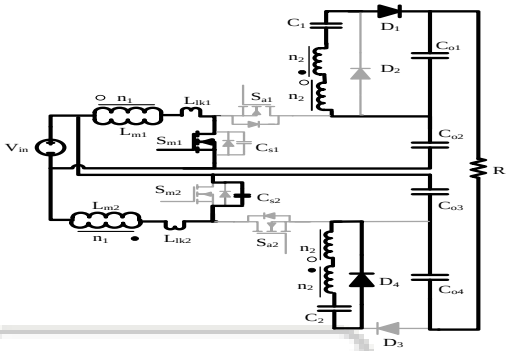


Fig. 12: Mode 7

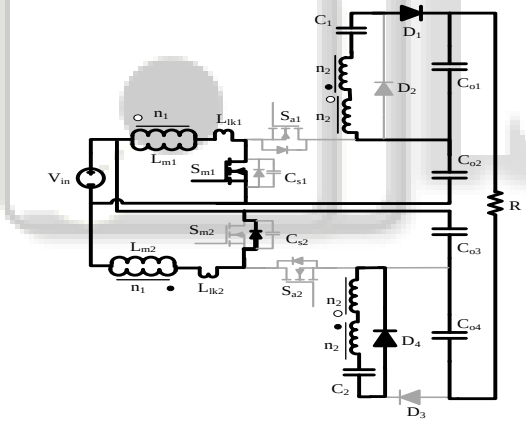


Fig. 13: Mode 8

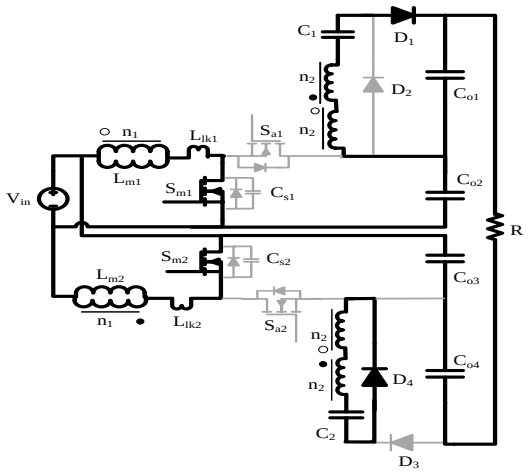


Fig. 14: Mode 9

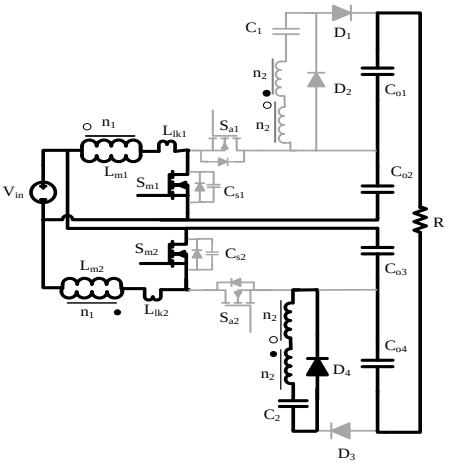


Fig. 15: Mode 10

III. DESIGN EQUATIONS

A. Voltage gain

Applying volt-sec balance across magnetizing inductor

$$M = \frac{V_o}{V_{in}} = \frac{4N + 1 + D}{1 - D}$$

From above equation the voltage gain is large even if N=1. So, moderate duty cycle (D) can be used in proposed converter as compared to conventional boost converter which can reduce input and output current ripple.

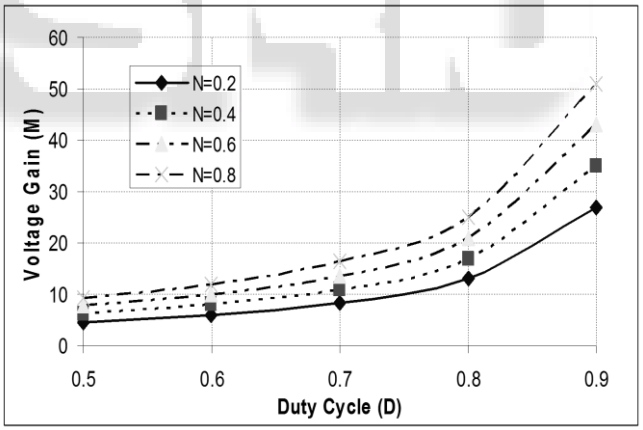


Fig. 16: Voltage gain

B. Voltage stress of semi-conductor devices

The filter capacitor of a conventional boost converter itself acts as clamping capacitor, which is large enough to suppress the switch turned off voltage spike

$$V_{sm1,\,stress} = V_{sm2,\,stress} = V_{co2} = \frac{1}{1-D} V_{in}.$$

$$V_{sa1,\,stress} = V_{sa2,\,stress} = V_{co2} = \frac{1}{1-D} V_{in}$$

From (15) and (16) voltage stress of power switches can be controlled by controlling duty cycle and transformer turns ratio. So, low voltage and high

performance device can be used to reduce switching and conduction losses.

C. Zero current Switching of Diodes

Because of auxiliary active clamping circuit all semiconductor switches are turned on with ZVS due to which switching losses are reduced. Also, all the diodes are turned off using ZCS due to presence of leakage inductance in coupled inductor.

$$\frac{di_{D1}(t)}{dt}+\frac{di_{D4}(t)}{dt}\approx\frac{V_{co3}}{2N*L_{lk}}$$

$$\frac{di_{D2}(t)}{dt}+\frac{di_{D3}(t)}{dt}\approx\frac{V_{co2}}{2N*L_{lk}}$$

D. power device selection

Assuming the clamp capacitor is large enough to suppress the voltage spike caused by the leakage inductor, the voltage stress of main and auxiliary switch is given by

$$V_{sm1,\,stress}=V_{sm2,\,stress}=\frac{1}{1-D}V_{in}$$

$$V_{sa1,\,stress}=V_{sa2,\,stress}=\frac{1}{1-D}V_{in}$$

E. Leakage Inductor Design

The leakage inductance has a direct influence on the diode turn off current falling rate;

$$L_{lk}\approx\frac{V_{co3}}{2N\left[\frac{di_D(t)}{dt}\right]}$$

Where, $i_D(t)$ is the total secondary current flowing through output diodes.

F. Capacitors Selection

In this converter, the clamp capacitor and filter capacitor of conventional boost are integrated. This capacitor is designed to minimize output voltage ripple and suppress the switch turn off voltage spike and to avoid excessive resonant ringing [17] due to parasitic elements of the power switch and transformer. A capacitor value is selected so that one half of resonant period exceeds the maximum turn off time of main switches.

$$C_{o2}\geq C_{o3}\geq\frac{(1-D_{\min})T^2}{\pi^2*L_{lk}}$$

1) Controller Design

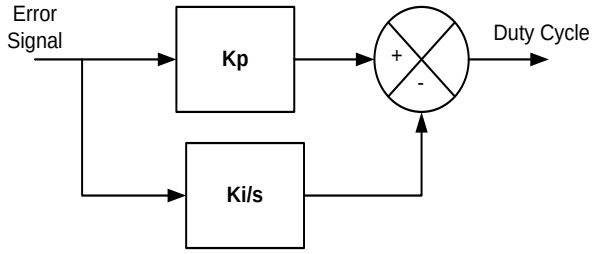


Fig. 17: Controller Design

The Pi Controller for the Converter has to be tuned such that the output voltage should not be varied under different input voltage and different load conditions. The soft switching performance of the converter also should not be affected by those disturbances.

The proposed values for Kp, Ki are given by

Kp=0.31

Ki=1/2.65e-4

IV. SIMULATION RESULTS

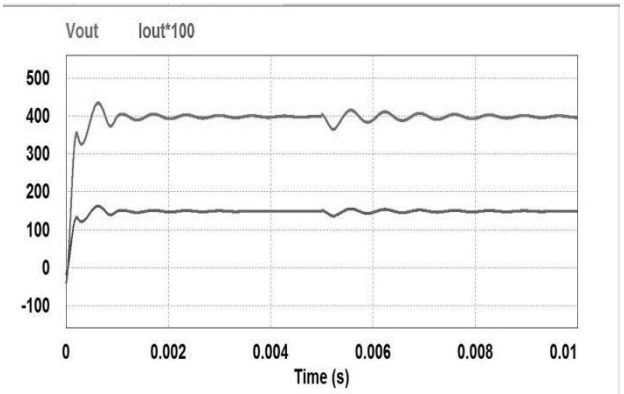


Fig. 18: Output Voltage and Current Wave forms with Input Voltage disturbance(Y-axis: voltage 100V/div, Current 1A/div)

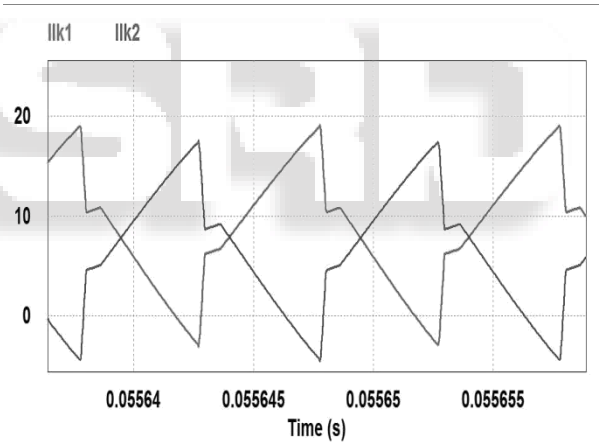


Fig. 19: Ilk1 and Ilk2 at Full load and 40V input

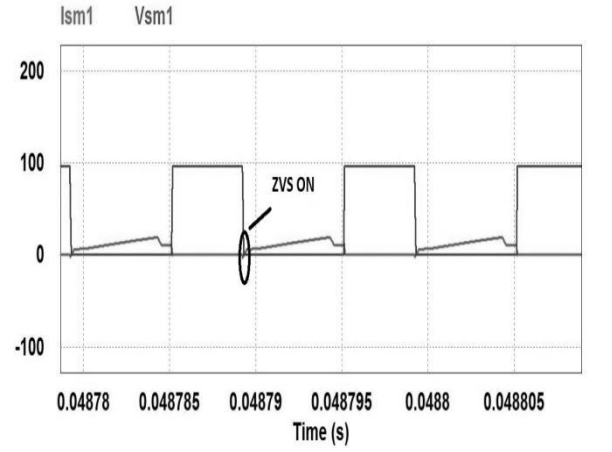


Fig. 20: Switch Voltage and Current waveforms(at Full load and 40V input)

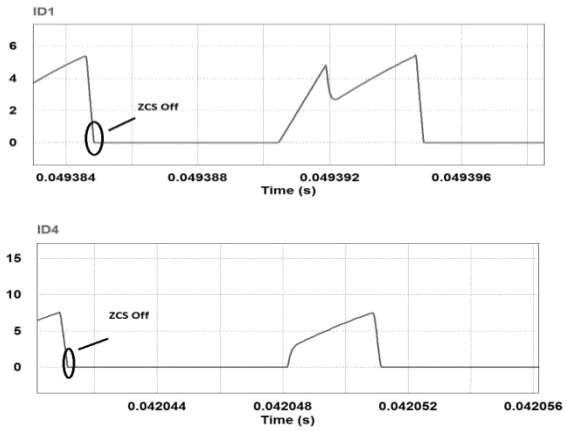


Fig. 21: Diode Currents ID1 and ID4 at Full load and 40V input

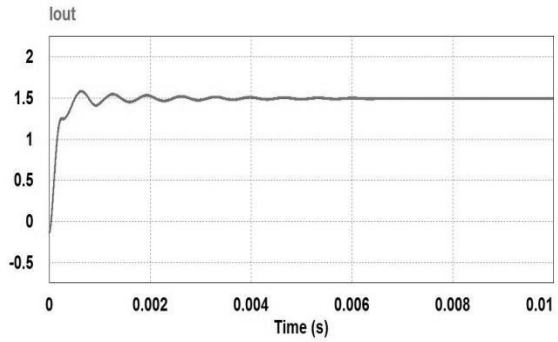


Fig. 22: Output current at Input Voltage 35V

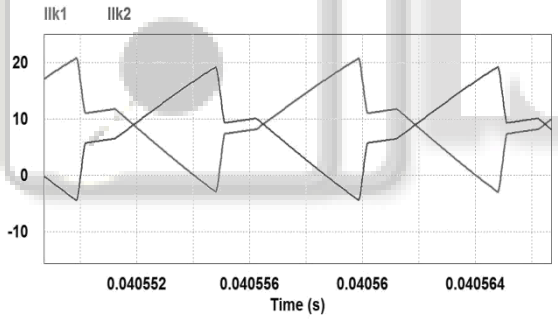


Fig. 23: Ilk1 and Ilk2 at input voltage 35V

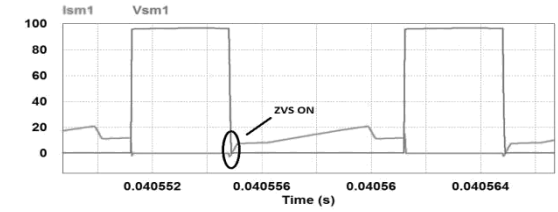
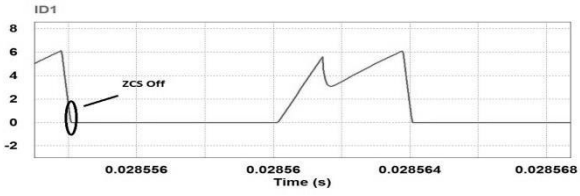


Fig. 24: Switch Voltage and Current at 35V input



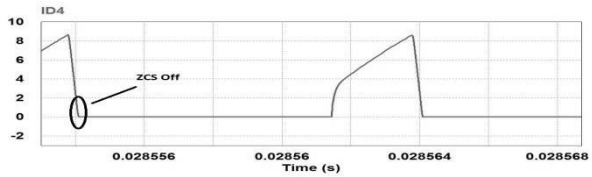


Fig. 25: Diode Currents ID1 and ID4 at 35 V input

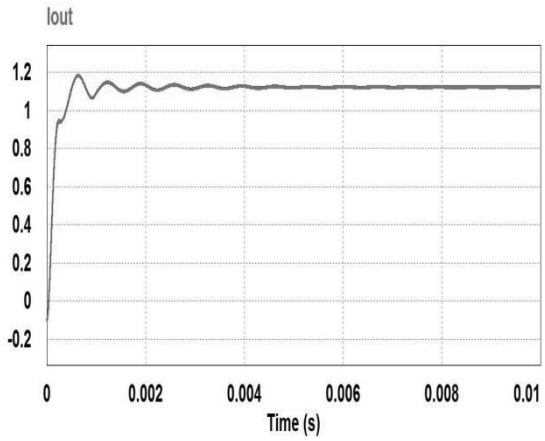


Fig. 26: Output Current at 3/4th of full load Condition

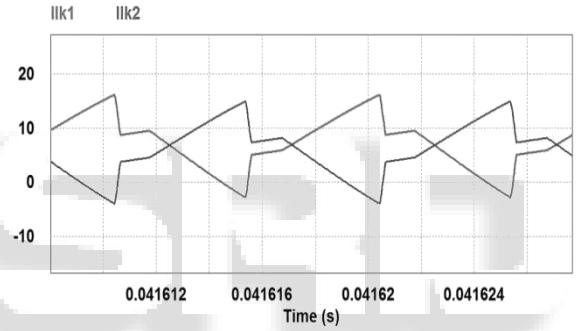


Fig. 27: Ilk1 and Ilk2 at 3/4th of full load Condition

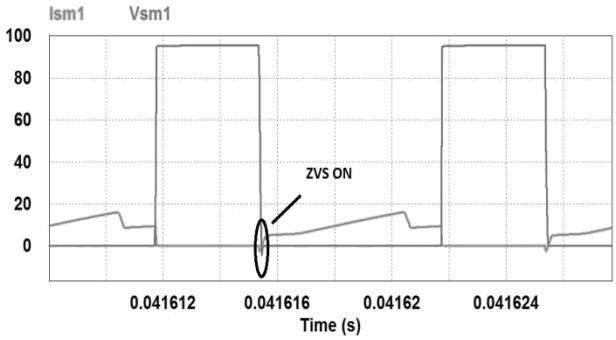
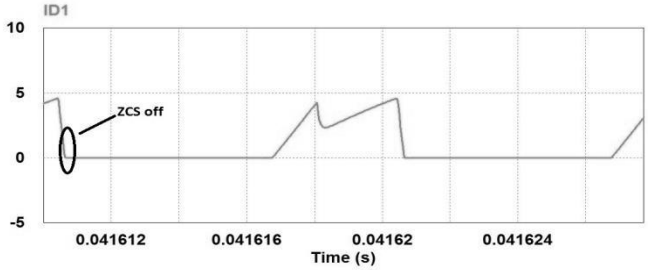


Fig. 28: Switch Voltage and Current at 3/4th of full load



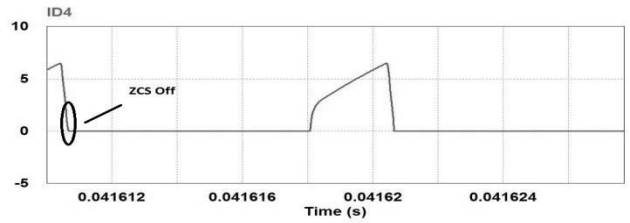


Fig. 29: Diode Currents ID1 and ID4 at 3/4th full load Condition

From the figure it can be observed that the output voltage is maintained constant even with the reduction of input voltage from 40V to 35V at time step 0.005sec.And also it can be stated that the converter will be maintaining the same output voltage for different input voltages(range 35-48V) and different load conditions which is quite important for renewable applications. The main switch is having Zero Voltage turn on and the output rectifier diodes are having Zero Current Turn off. The soft switching of the converter power semiconductor devices also achieved for different operating conditions using sophisticated controller parameters.

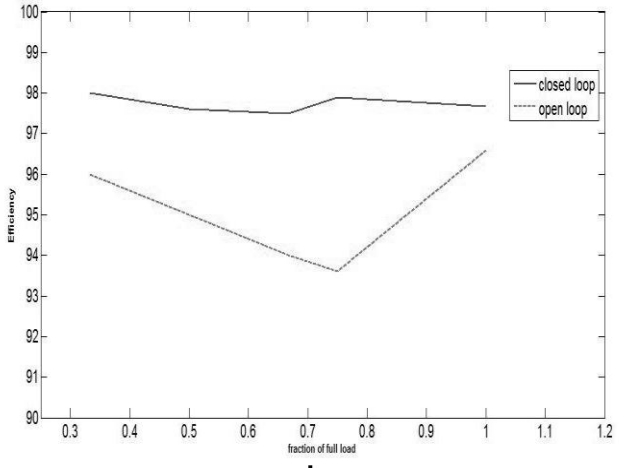


Fig. 30: Efficiency Vs Fraction of load curve

from the figure 4-1 the efficiency of the converter is high due to soft switching of power semiconductor devices and it is further improved in closed loop operation. The peak efficiency of the converter is 98% which is quite high in high gain topologies.

V. Conclusion

This paper presented 600w prototype of a soft switching high gain dc –dc converter and its closed loop operation is achieved. From this it is concluded that compared to other converter topologies it is having lesser input current ripple, optimal turns ratio of coupled inductors, and lesser size due to high frequency operation of the converter. Due to closed loop operation of the converter the efficiency is improved greatly and it is best suited for renewable applications.

References

[1] I.Barbi and R.Gules ,Isolated dc-dc converters with high output voltage with TWTA Telecommunication Satellite Applications," IEEE Trans. power electron.,vol.18,no.4,pp.975-984,July.2003

[2] K.C.Tseng and T.J.Liang," Novel high efficiency step up converter",proc.Inst.Elect.Eng.,vol.151,pp.182-190,2004

[3] N.Mohan, T.M.Undeland, and W.P.Robbins, power electronics: converters, Applications and Design.Newyork: Wiley, 1995.

[4] Zhao,Q.,Tao,F.,Hu,Y., and Lee,F.C.: 'Active Clamp Dc-Dc Converters using magnetic switches' Proc.Applied Power Electronics Conf.,2001,pp.946-952

[5] Lee,P.W., Lee,Y.S., Cheng,D.K., and Liu,X.C.: 'Steady state analysis of an interleaved boost converter with coupled inductors', IEEE Trans.Ind.Electron.,2000,8,(4),pp.787-795

[6] Wai, R.J., and Duane, R.Y.: 'High efficiency power conversion for low power fuel cell generation system', IEEE Trans .power Electron.,2005,7,(4),pp.847-856

[7] CALAISM. AGELIDISV.G., MEINHARDT.M. : 'Multilevel converters for single phase grid connected PV systems-an overview, sol. Energy, 1999, 66, (5), pp. 325- 335

[8] MARTINS A.S.,KASSICK E.V.,BARBI I.:' Control strategy of double boost converter in continuous conduction mode applied to power factor correction'. Proc.IEEE PESC,1996,pp.1066-1072

[9] BALOGH L., REDL R.: 'Power factor correction with interleaved boost converters in continuous inductor current mode'. proc. IEEE APEC,1993,pp.168-174

[10] DURAN-GOMEZJ.L.,GARCIA-CERVANTES E.,ENJETI P.N.,PALMA L.: 'Analysis and evaluation of a series-combined connected boost and buck-boost Dc-Dc converter for photo voltaic application, Proc.IEEE APEC,2006,pp.979-985

[11] ABUTBULO. GHERLITZA., BERCHOVICHY., IOINOVICI.: 'Step up switching mode converter with high voltage gain using a switched-capacitor circuit' ,IEEE Trans. circuits Syst.I, Fundam. Theory Appl., 2003, 50, (8), pp.1098-1102.

