# Design of an Efficient Sequential NANO-RAM Circuit using Reversible Gates

**S. Aathilakshmi[1] Mrs. R. Krishnaveni[2]**
[1]M.E Student [2]Assistant Professor
[1]Department of VLSI Design [2]Department of Electronics & Communication Engineering
[1,2]Kalaignar Karunanidhi Institute of Technology

*Abstract*— we proposed the Reversible logic, it is emerging technique for decrease the energy consumption for low power VLSI application such as QCA nanotechnology and many other computing technique. In existing large number of works done in irreversible combinational logic, but the design of combinational circuits power dissipation was high, to overcome this sequential reversible circuits designed by using flip flops, latches and combinational gates. The main purpose of designing reversible logic is to decrease the quantum cost, number of garbage ouputs.in this paper we have proposed a new reversible Nano-RAM circuit that is parity preserving reversible RAM circuit .The new reversible gates are Feynman double gate, new fault tolerant, memory cells, the proposed double edge triggered flip flop is compared with existing flip flops and its efficiency shown in power, gate count, garbage output. The simulation is verified using Xilinx 8.1 and implemented in FPGA.

***Key words:*** Reversible Logic, Nano-RAM, Parity Preserving, Gate Count, Garbage Output, NFT, and Double Edge Triggered flip flop, Nanotechnology, VLSI Design, Fault Tolerance System, Quantum Computing, Low Power Design

## I. INTRODUCTION

Mozammel h a khan[1] states that Reed Muller expression is used to design the reversible sequential 4bit level triggered counter registers.in this the gate count, garbage output energy consumption was increased and restricted number of fan out was used.so we proposed the Nano-RAM circuit, it is very efficient to avoid energy losses.landatuer[2] described that high technology circuits and system constructed using irreversible combinational logic circuit produce lots of heat dissipation compare to proposed work.in that we proposed reversible sequential circuits, demonstrated that the loss of information dissipates ktln2 joules of energy where k is Boltzmann's constant and t is the absolute temperature. Heat dissipation is avoided using the reversible gates. Bennett states that heat dissipation and energy loss avoided in reversible logic[3],but the more number of area required for the combinational circuit, to achieve this the reversible sequential logic is used to one to one mapping, input is achieved by output vector.in reversible gate one of the main parts of electronic device is memory. Efficient design of memory to improve the efficiency of electronic devices. One of the main objectives of reversible gate is reduce the power loss. The reversible gate have many advantages, important in energy consumption, used to design efficient memory, according to the memories, random access memory is an very crucial part in electronic circuit, systems in particular. Some of them have been achieved, importance of reversible technology for designing of random access memory(RRAM),now to extend this work using parity preserving reversible random access memory[4], parity preserving is important for checking the fault. The main elements in the RAM circuits are mux, decoder, Feynman double gate, new fault tolerant gate, double edge triggered flip flop have been designed. The designing compare with existing work and the efficiency is shown. Reversible gate has many application in many emerging computing technologies such as SFL technology [5], [6], optical technology, quantum dot cellular automata technology, and nanotechnology [7]. Moreover, reversible logic is a most popular in quantum computing and quantum information [8]. In summary, reversible logic has become a promising technology for power efficient emerging computing technologies.

## II. REVERSIBLE GATE DESCRIPTION

### A. *Reversible Gate:*

Equal number of gates present in both input and output in that input vector is related to the output vector that is IV=(i1,i2,i3….in) and OV=(o1,o2,o3…on). A reversible gate can be denoted as NxN, it introduce both input and outputs equal.it is like a feedback form, so the main advantage is reduction of time and energy loss.

### B. *Garbage Output:*

A garbage output is an unused output that is added to change an irreversible gate to a reversible one and not used for the next stage output. It is applicable for reversible gate in that some outputs. Then, a extremely great number number of garbage outputs are not proper. The large number of garbage output needed to change a irreversible gate to a reversible one is log2n in which n is the iteration of specific pattern in an output.

### C. *Quantum Gate:*

Quantum gates are related to quantum computing that is gate count and reversible gates. We can use quantum technique for identifying 1×1 and 2×2 quantum gates. Since larger gates such as 3×3 cannot be justified by quantum technique straight ,so simple quantum gates are used for identifying larger quantum gates such as 3,4 IV and OV etc..,

### D. *Quantum Cost:*

Many of them methods used for computing of gate count of quantum circuits or reversible circuits. In simple terms, quantum cost is the number of 1×1 and 2×2 quantum gates is used in quantum circuits or reversible circuits.

## III. TYPES OF REVERSIBLE GATES

Many reversible gates have been shown,the basics are NOT gate, CNOT gate (FG), Toffoli gate (TG), Peres gate (PG), NFT gate, PH3 gate. There are several basic gates which can

 

be used for understanding the reversible gates and it circuits. Such as NOT, CNOT-v, CNOT v+ and Feynman gate. Since the quantum cost of basic gates is taken unity, thus, they are used for computing of quantum cost of reversible circuits.

*A. NOT Gate:*

The quantum implementation of NOT gate is shown in Fig.1. NOT gate is a 1×1 reversible gate and its quantum cost is same. It should be noted that Controlled-V is a square-root-of NOT gate and V+ is its hermitian that is the pair of matrix elements.


Fig. 1: NOT gate

*B. CONTROLLED-NOT GATE (CNOT):*

Feynman gate is a 2×2 reversible gate and Also known as CNOT gate. The basic diagram and quantum implementation of Feynman gate is represented in Fig. 2(a) and 2(b).Therefore, FG can be used to copy a signal in reversible circuits.

In way that if input vector of FG is quantified IV= (A, 0), the output vector of circuit will be OV= (A, A), represented in Fig. 2(c).

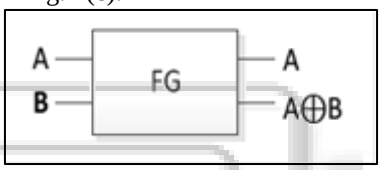


Fig. 2(a): Feynman gate

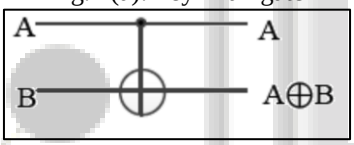


Fig. 2(b): Quantum implementation of Feynman

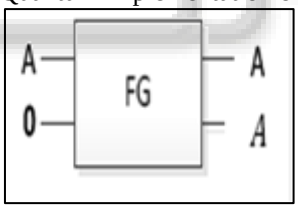


Fig. 2(c): Symbol of Feynman gate

*C. Parity Preserving Reversible Gates:*

In these types of reversible gates, the parity of input and output is the same, and also used for the error detection put it simply, XOR of input and output vector are equal. Parity preserving reversible gate is a fault tolerant reversible gate. Some of the parity preserving reversible gate is Feynman double gate (F2G) new fault tolerant gate (NFT) which has been used in this work, represented in fig. 3, 4 respectively. Parity preserving reversible gate is used for designing of PPRNRAM, therefore, F2G and NFG is used to make copy a signal and perform of and operation similarly. Quantum cost of F2G is 2 and NFG is 5.

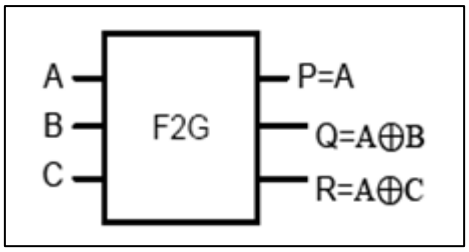


Fig. 3: Feynman double gate (F2G)

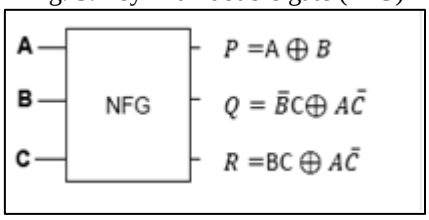


Fig. 4: New Fault Tolerant Gate (NFT)

*D. Traditional Reversible Gates:*

The fault tolerant reversible gates, not only in parity preserving gates, the equal number of input and output parity, but also have an equal pair weight. Different aspects, in conservative reversible gate both the number of ones in input and output are unique. It's clear that the conservative gates are a parity preserving, but different. FRG is one of the few conservative gates have been introduced in the reference which have been utilized in this work and shown in fig. 5. Quantum cost of FRG is 5.

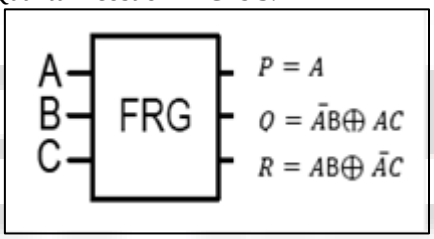


Fig. 5(a): Fredkin gate

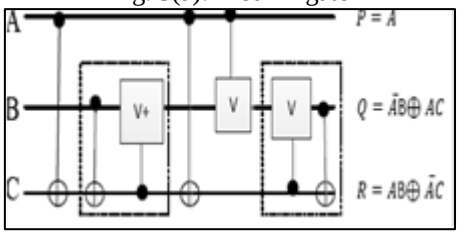


Fig. 5(b): Quantum implementation of frg

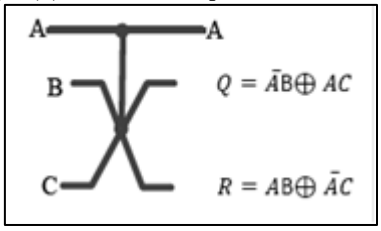


Fig. 5(c): Symbol of frg

## IV. NANO-RAM DESCRIPTION

The electronic circuit was designed using many of the component in this the memory element is very important.it is used to store the different types of data, to reduce the energy consumption.in memory element RAM is high efficiency, in that NANO-RAM is advanced and avoid loss of data. We proposed the NANO-RAM reversible gates. Reversible gate is used for energy saving, in recent trends

 

parity preserving reversible Nano random access memory is proposed (PPRNRAM).

### *A. Parity Preserving Reversible Multiplexer:*

Two input multiplexer is done in [11] now it can be used to extend a general design of multiplexer. The 4×1 multiplexer is shown in Fig. 6, described in [9].

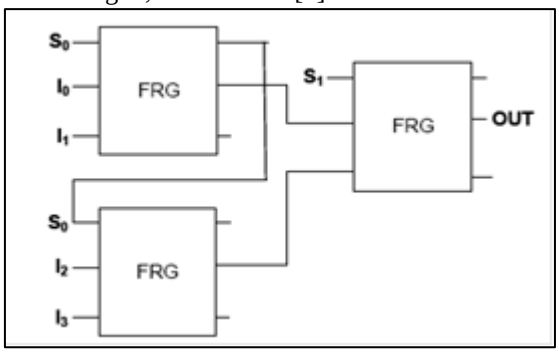


Fig. 6: parity preserving 4x1 mux

the mux is used in output part, it is used to produce multiple into a single output.in that 4x1 mux is proposed,3 reversible gates and 5 garbage outputs in which n is 4 and m is 2,quantum cost is 5.

### *B. Parity Preserving Reversible Decoders:*

In existing 1x2 decoder is designed using simple Feynman gate [10], now we proposed parity preserving decoder using Feynman double gate.The reversible 1×2 decoder design is shown in Fig. 7 and a parity preserving decoder is shown in Fig. 8.

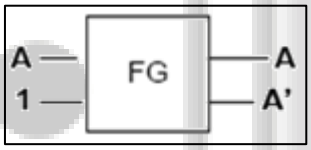


Fig. 7: Reversible 1x2 decodrer

For designing a 2×4 decoder, the design of 1×2 decoder is used in that 1×2 decoder has been used as primary input for the two reversible FRG gates. Fig.9 shows 2×4 decoder design. In F2G two outputs of a and ~a is available and these two outputs merge with B input and FRG gate and give forth ~ (AB), ~AB, A~B and AB. On the basis of 2×4 decoder, a similar design can be used to extend the reversible decoder of . The achieved design, based on a F2G and FG parity preserving gate.

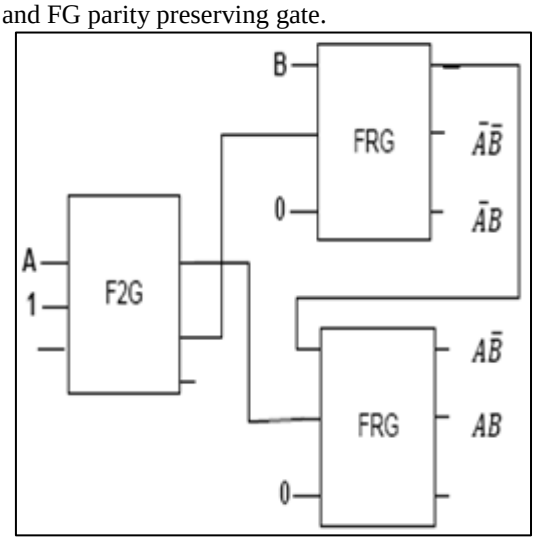


Fig. 8: parity preserving 2x4 decoder

## V. DESIGN OF NANO RAM CIRCUIT

Complete this entire works to merging these parts. The basic decoder concept is to produce n input to a power of 2 n outputs. We proposed 2x4 decoder for the parity preserving design, and Feynman double gate is used to extend from the Feynman gate, it is used for the simple gate design to reduce the power in circuit design. The new fault tolerant gate is used to tolerate the faults that are used to check the inputs and provide the output for the possible input, without any error. The master slave d flip flop is used as memory element, but at a time it is act master or slave to overcome this we proposed Double Edge Triggered flip flop, it is very efficient for both positive and negative edge triggered flip flop. The mux is used to produce multiple inputs into single output. Main advantage is reduce the area, so we proposed 4x1 multiplexer.this is the works done in the proposed Nano- RAM block.

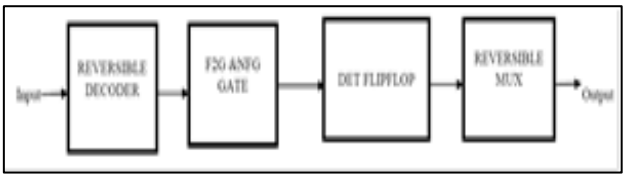


Fig. 9: NANO RAM BLOCK DIAGRAM

## VI. SIMULATION RESULT

| Power summary: | I(mA) | P(mW) |
|---|---|---|
| Total estimated power consumption: | | 29 |
| | | |
| Vccint 1.20V: | 9 | 11 |
| Vccaux 2.50V: | 7 | 18 |
| Vcco25 2.50V: | 0 | 0 |
| | | |
| Inputs: | 4 | 4 |
| Logic: | 0 | 0 |
| Outputs: | | |
| Vcco25 | 0 | 0 |
| Signals: | 0 | 1 |
| | | |
| Quiescent Vccint 1.20V: | 5 | 6 |
| Quiescent Vccaux 2.50V: | 7 | 18 |

Fig. 10: Power summary of NANO-RAM circuit

| Device Utilization Summary | | | | |
|---|---|---|---|---|
| Logic Utilization | Used | Available | Utilization | Note(s) |
| Number of 4 input LUTs | 5 | 1,536 | 1% | |
| Logic Distribution | | | | |
| Number of occupied Slices | 3 | 768 | 1% | |
| Number of Slices containing only related logic | 3 | 3 | 100% | |
| Number of Slices containing unrelated logic | 0 | 3 | 0% | |
| Total Number of 4 input LUTs | 5 | 1,536 | 1% | |
| Number of bonded IOBs | 12 | 97 | 12% | |
| Total equivalent gate count for design | 30 | | | |
| Additional JTAG gate count for IOBs | 576 | | | |

Fig. 11: design summary of NANO-RAM circuit

| Existing and proposed work | Power | Gate count | Garbage outputs |
|---|---|---|---|

 

| | | | |
|---|---|---|---|
| Reed Muller existing work | 67 mw | 60 | 17 |
| NANO-RAM circuit proposed work | 29 mw | 30 | 9 |

Table 1: Comparison between Existing and Proposed Work

## VII. CONCLUSION

In this work, a new parity preserving reversible RAM is designed using the component such as mux, decoder and flip flop are proposed in parity preserving reversible gates. Designs were compared with existing works and efficiency of design in gate count, garbage output is shown.DET is used to reduction of power losses, the proposed DET flip flop is compared with existing work and its efficiency in gate count and garbage output is shown. The simulation result done using Modelsim10.1 and Xilinx 8.1.

### *A. Future Work:*

In future work the proposed NANO-RAM is applying in MAC unit with sufficient modification. And also compared the existing master slave with proposed double edge triggered flip flop using QCA tool.

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