Low Area and High Speed Vedic Mathematics Multiplier using Compressor

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Abstract— There is a growing demand for high speed processing and low area design for VLSI and Communication applications in recent days. The integral part of the processor is the multiplier. The multiplier is designed using compressors. The compressors used are 4:2, 5:2, 7:2 compressors. The compressors are designed using full adder and half adder. The multiplier design is based on Urdhwa Tiryakbhayam sutra. The developed model is designed using microwind and DSCH software. The proposed multiplier has reduces the area and power consumption.

Key words: urdhwa tiryakbhyam sutra, 4:2 compressor, 5:2 compressor, 7:2 compressor

I. INTRODUCTION

In this paper we proposed an 8-bit multiplier using a Vedic mathematics (Urdhwa Triyakbhyam sutra) for generating the partial products. The partial product addition in Vedic multiplier is realized using carry skip technique reduce the number of logic levels. An 8-bit multiplier is realized using a 4-bit multiplier and modified ripple carry adder [1]. Architecture to perform high speed multiplication using ancient Vedic math's technique is proposed. To increase the speed of multiplier the half adder and full adder of the Vedic mathematics multiplier is replaced with compressor. In this 4:2 compressors are used for adding more than 3bits at a time [2]. In this paper Vedic mathematics technique based multiplier uses 4:3, 5:3, 6:3 and 7:3compressors for addition. The designs were analyzed in Cadence RTL compiler in 180nm technology. In this higher order compressor for used to design an 8*8 multiplier. It can be used in low area and power critical applications [3]. In this symbol CMOS 4:2 compressor using pass logic is develop. This circuit is design using an X-OR and X-NOR combination gates it eliminates the use of inverters.

The total circuit consists of 28 transistors [4]. In this paper a new high speed multiplier is designed is using 4:2 and 7:2 compressors for addition. This technique in two times faster than the ancient multiplier technique. The multiplier was designed using Xilinx Spartan 3e series of FPGA [5]. In this paper a new technique is proposed to perform 8*8 multiplications. The multiplier is designed using the combination of half adder, full adder, 4:2compressor, 5:2, and 7:2 compressors. This technique requires low area, high speed and is a very efficient technology.

II. METHODOLOGY

A. Vedic Maths Urdhwa Tiryakbhyam Sutra:

There are 16 different sutras to perform mathematical calculations in Vedic mathematics. The highly preferred algorithms to perform calculation are Urdhwa Tiryakbhyama Sutra. It is originated from two Sanskrit words Urdhwa and Tiryakbhyam means vertically and crosswise. It can be used for the multiplication of integers as well as the binary numbers. It uses full adder, half adder, 4:2, 5:2, and 7:2 compressors to perform multiplication. Let us consider two 8 bit numbers A_7-A_0 and B_7-B_0 where 0 is the least significant bit (LSB) and 7 is the most significant bit (MSB).The products obtained are P_0-P_{15} and the partial products are calculated using logical AND operation.

$P_0 = A_0*B_0$

$C_1P_1 = (A_1*B_0) + (A_0*B_1)$

$C_3C_2P_2 = (A_2*B_0) + (A_1*B_1) + (A_0*B_2) + C_1$

$C_5C_4P_3 = (A_3*B_0) + (A_2*B_1) + (A_1*B_2) + (A_0*B_3) + C_2$

$C_7C_6P_4 = (A_4*B_0) + (A_3*B_1) + (A_2*B_2) + (A_1*B_3) + (A_0*B_4) + C_3 + C_4$

$C_{10}C_9C_8P_5 = (A_5*B_0) + (A_4*B_1) + (A_3*B_2) + (A_2*B_3) + (A_1*B_4) + (A_0*B_5) + C_5 + C_6$

$C_{13}C_{12}C_{11}P_6 = (A_6*B_0) + (A_5*B_1) + (A_4*B_2) + (A_3*B_3) + (A_2*B_4) + (A_1*B_5) + (A_0*B_6) + C_7 + C_8$

$C_{16}C_{15}C_{14}P7 = (A_7*B_0) + (A_6*B_1) + (A_5*B_2) + (A_4*B_3) + (A_3*B_4) + (A_2*B_5) + (A_1*B_6) + (A_0*B_7) + C_9 + C_{11}$

$C_{19}C_{18}C_{17}P_8 = (A_7*B_1) + (A_6*B_2) + (A_5*B_3) + (A_4*B_4) + (A_3*B_5) + (A_2*B_6) + (A_1*B_7) + C_{10} + C_{12} + C_{14}$

$C_{22}C_{21}C_{20}P_9 = (A_7*B_2) + (A_6*B_3) + (A_5*B_4) + (A_4*B_5) + (A_3*B_6) + (A_2*B_7) + C_{13} + C_{15} + C_{17}$

$C_{25}C_{24}C_{23}P_{10} = (A_7*B_3) + (A_6*B_4) + (A_5*B_5) + (A_4*B_6) + (A_3*B_7) + C_{16} + C_{18} + C_{20}$

$C_{27}C_{26}P_{11} = (A_7*B_4) + (A_6*B_5) + (A_5*B_6) + (A_4*B_7) + C_{19} + C_{21} + C_{23}$

$C_{29}C_{28}P_{12} = (A_7*B_5) + (A_6*B_6) + (A_5*B_7) + C_{22} + C_{24} + C_{26}$

$C_{31}C_{30}P_{13} = (A_7*B_6) + (A_7*B_6) + C_{25} + C_{27} + C_{28}$

$C_{32}P_{14} = (A_7*B_7) + C_{29} + C_{30}$

$P_{15} = C_{31} + C_{32}$

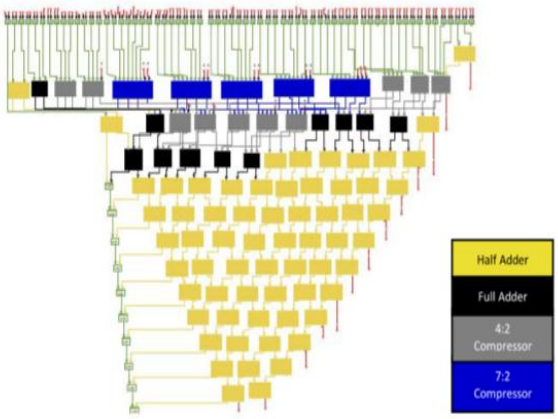

Fig. 1: Compressor based multiplier

B. Adder Design:

To increase the speed of the addition of 4 bits at a time a compressor adder is used the speed and performance of the processor is increased by replacing the several half and full adders with compressor. The compressor adder used in this is 4:2, 5:2 and 7:2 compressors.

1) 4:2 Compressors:

A 4:2 compressor black box is shown in figure 2, is capable of adding 4 bits and one carry and produce a 3bit output. The 4:2 adder using full adder and half adder to add 5 bits is given in fig 3. And it has one full adder 4 half adder and one XOR gate.

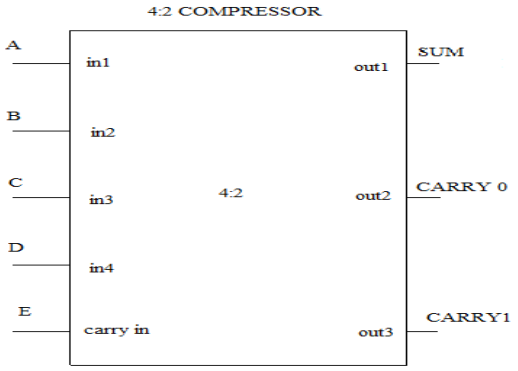

Fig. 2: Black box representation of 4:2 compressor

INPUT	OUTPUTS		
NO OF INPUTS HIGH	CARRY 1	CARRY 0	SUM
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

Table 1: Truth table of 4:2 compressor

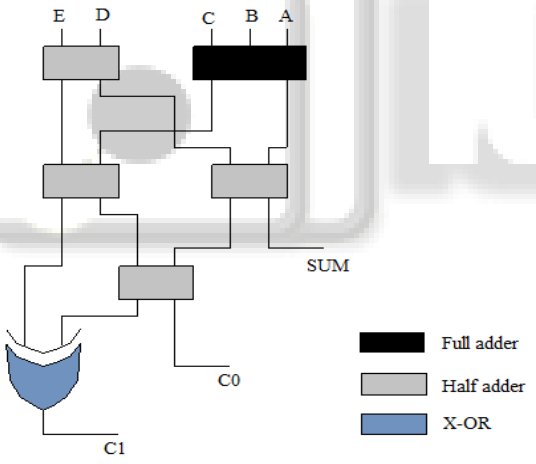

Fig. 3: Existing architecture of 4:2 compressor

The design is reduced by using 2 full adders and one half adder as shown in fig 4.

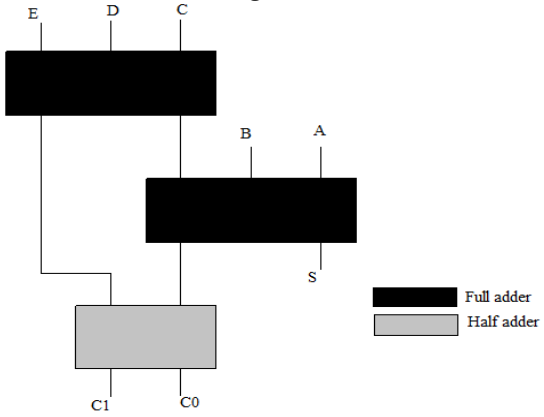

Fig. 4: Proposed architecture of 4:2 compressor

2) 5:2 Compressor:

This adder is based on full adder and half adder. It is used to add more than 5 bits at a time. The black box representation of the compressor adder is given in fig 5. There are 7 inputs to the adder in which 5 bits are normal inputs and 2 are carry bits and it produces 3 bit output. The 5:2 compressor adder uses 4 full adders only. The compressor is shown in fig 6.

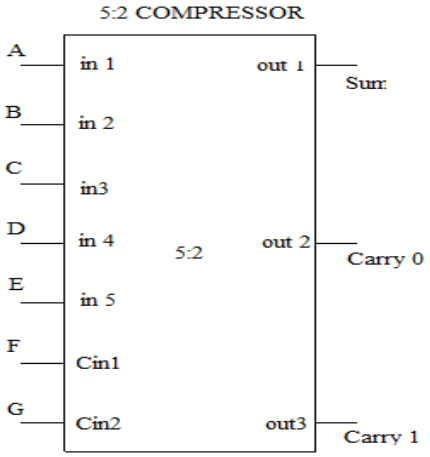

Fig. 5: Black box representation of 5:2 compressor

INPUT	OUTPUTS		
NO OF INPUTS HIGH	CARRY 1	CARRY 0	SUM
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table 2: Truth table for 5:2 compressor

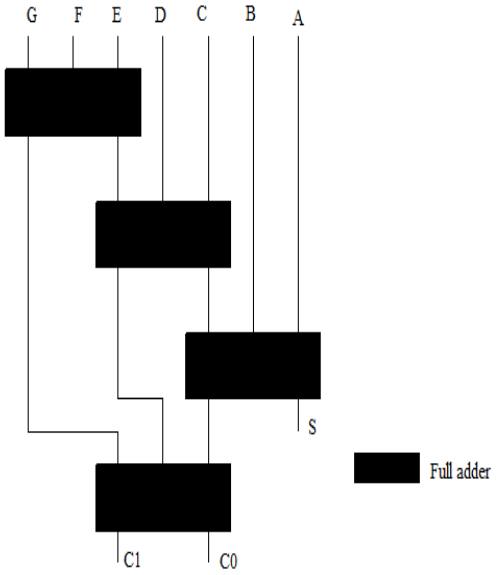

Fig. 6: Architecture of 5:2 compressor

3) 7:2 Compressor:

The compressor adder is a capable of adding 7 bits of input and 3 carry bits. It utilizes two 4:2 compressors, one half adder and two full adder. It is used to add more than 7 bits. The black box representation is shown in fig 7.

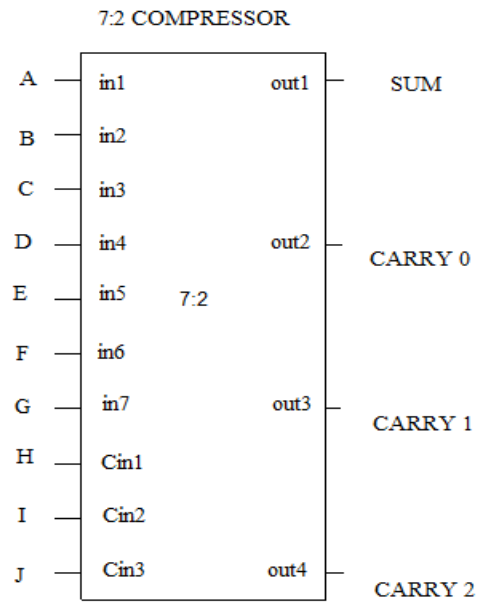

Fig. 7: Black box representation of 7:2 compressor

INPUT	OUTPUTS			
NO OF INPUTS HIGH	CARRY 2	CARRY 1	CARRY 0	SUM
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0

Table 3: Truth table of 7:2 compressor

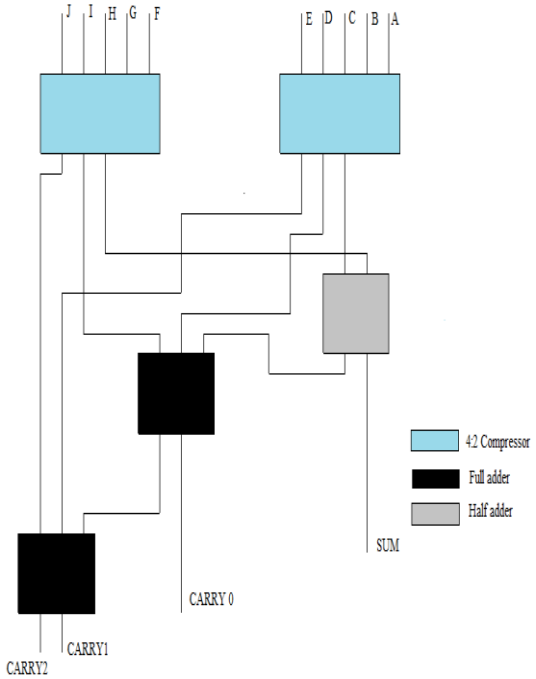

Fig. 8: Architecture of 7:2 compressor

There are four outputs with one sum and 3 carry. The design of the 7:2 compressor is shown in fig 8.

III. Result and Discussion

The architecture of compressor based multiplier is shown in fig 9. The multiplier is designed using microwind software. The proposed model of compressor has one half adder and full adder, one OR gate, three 4:2 compressors, three 5:2 compressors and six 7:2 compressors. It can be used to multiply two 8-bit binary number. The input to the design is A_7-A_0 and B_7-B_0 and the output is P_0-P_{15}. The proposed technique reduces the area to 40% and increases the efficiency.

Existing system			Proposed system		
		Total			Total
AND gate	64	74	AND gate	64	65
EX-OR gate	10		OR gate	01	
Half Adder	64	75	Half Adder	01	02
Full Adder	11		Full Adder	01	
4:2 Compressor	10	15	4:2 Compressor	03	12
5:2 Compressor	00		5:2 Compressor	03	
7:2 Compressor	05		7:2 Compressor	06	

Table 4: Comparison table for existing vs proposed system

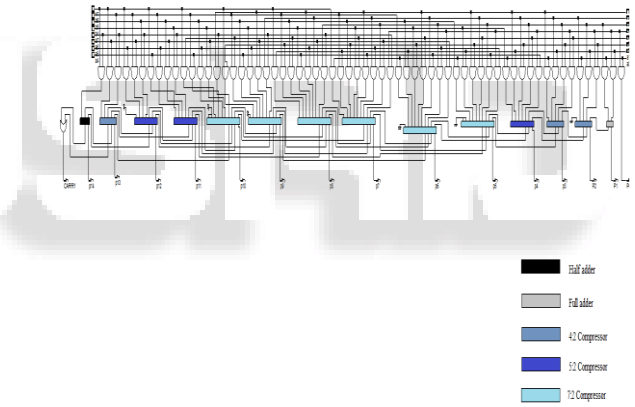

Fig. 9: Proposed architecture of multiplier using compressors

IV. Conclusion

In this paper a novel simplified 8*8 compressor is designed using microwind and the performance is analysed. The compressor produces very efficient output and reduces the area compared to the conventional methods.

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