# A Simulation of 3 Levels and 5 Levels Diode Clamp (NPC) Inverter and it's Comparison

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*Abstract*---In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. They can generate output voltages with extremely low distortion and lower dv/dt, they draw input current with very low distortion, they generate smaller common mode voltage and they can operate with a lower switching frequency. Because of these features worldwide research and development of multilevel inverters is occurring. In this report the simulation results and its comparison of diode clamped 3 levels and 5 level inverter has been shown.

***Key words***: control strategies, three and five level simulation, and FFT analysis.

## I. Introduction To Multilevel Inverter

### A. *Principle of Multi-level inverter*

If the DC voltage sources are connected in series, it becomes possible to generate an output voltage with several steps. Multilevel inverters include an arrangement of semiconductors and DC voltage sources required to generate a staircase output voltage waveform. Figure 1. Shows the schematic diagram of voltage source-inverters with a different number of levels. It is well known that a two level inverter, such as the one shown in Figure1.1, generates an output voltage with two different values (levels) $V_c$ and "zero", with respect to the negative terminal of the DC source ("0"), while a three level module, Figure1.2 generates three different voltages at the output ($2V_c$, $V_c$ and "zero"). The different positions of the ideal switches are implemented with a number of semiconductors that are in direct relation with the output voltage number of levels. Multilevel inverters are implemented with small DC sources to form a staircase ac waveform, which follows a given reference template. For example, having ten DC sources with magnitudes equal to 20 V each a composed m-level waveform can be obtained (five positive, five negatives and zero with respect to the middle point between the ten sources), generating a sinusoidal waveform with 100 V amplitude as shown in Fig.1.2: and with very low THD.

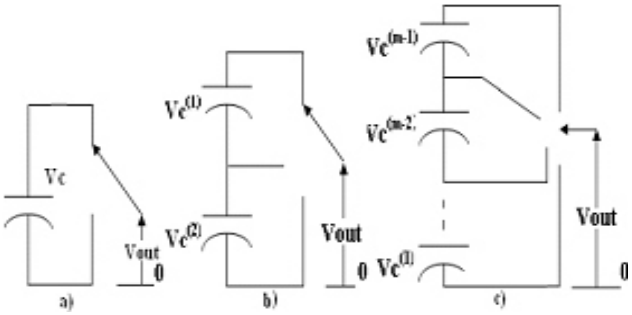



Fig.1: Diagram of Two, Three & m-Level Inverter

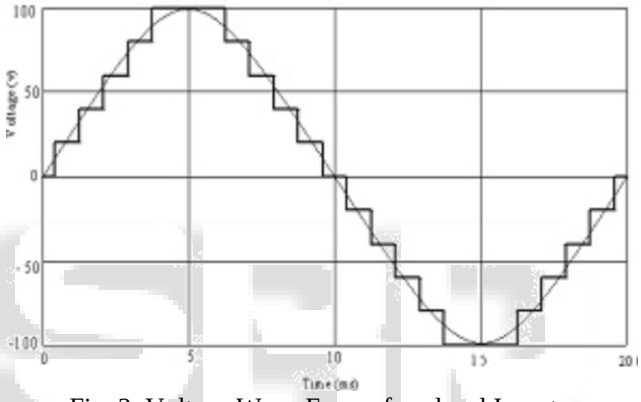



Fig. 2: Voltage Wave Form of m- level Inverter

### B. *Different Topologies of Multilevel Inverter:*

Different topologies of multilevel inverter are discussed besides:

1. Diode-Clamped Inverter
2. Flying Capacitor Multilevel Inverter
3. Capacitor-Clamped Inverter
4. Cascaded Multicell Inverters
5. Generalized Multilevel Cells

### C. *Diode Clamped Multilevel Inverter:*

A three-level diode-clamped inverter is shown in Fig 3.1(a) in this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors $C_1$ and $C_2$. The middle point of the two capacitors can be defined as the neutral point.

The output voltage van has three states: $V_{dc}/2$, 0,-$V_{dc}/2$. For voltage level $V_{dc}/2$ switches $S_1$ and $S_2$ need to be turned on; for $-V_{dc}/2$ , switches$S_1$' and $S_2$' need to be turned on; and for the 0 level,$S_2$ and $S_1$' need to be turned on.

The key components that distinguish this circuit from a conventional two-level inverter are $D_1$ and $D_1$' which clamp the switch voltage to half the level of the dc-bus voltage. When both $S_1$ and $S_2$ turn on, the voltage across a and 0 is $V_{dc}$, i.e., va0=$V_{dc}$. In this case $D_1$', balances out the voltage sharing between $S_1$' and $S_2$' with $S_1$' blocking the

voltage across $C_1$ and $S_2$' blocking the voltage across $C_2$. Notice that output voltage $v_{an}$ is ac, and $v_{a0}$ is dc. The difference between $v_{an}$ and $v_{a0}$ is the voltage across $C_2$, which is $V_{dc}/2$.

If the output is removed out between aand 0, then the circuit becomes a dc/dc converter, which has three output voltage levels: $V_{dc}$, $V_{dc}/2$, and 0. Fig. 3.2(b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, $C_1$, $C_2$, $C_3$, and $C_4$. For dc-bus voltage $V_{dc}$, the voltage across each capacitor is, $V_{dc}/4$ and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes.

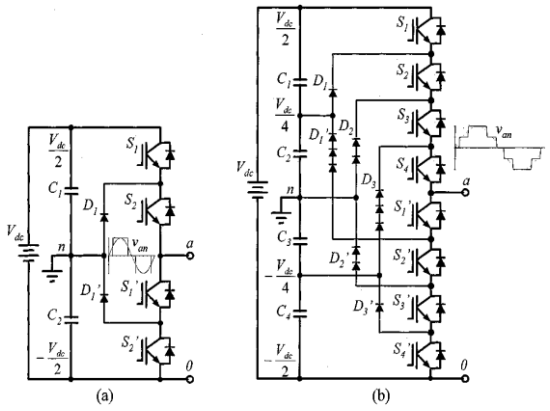



Fig. 3: (a)-3 level diode clamp inverter (b)-5 level diode clamp inverter

There are five switch combinations to synthesize five level voltages across a and n-

1) For voltage level $V_{an} = V_{dc}/2$, turn on all upper switches $S_1$–$S_4$.
2) For voltage level $V_{an} = V_{dc}/4$, turn on three upper switches $S_2$–$S_4$ and one lower switch S1'.
3) For voltage level $V_{an} = 0$, turn on two upper switches $S_3$ and $S_4$ and two lower switches $S_1$'and $S_2$'.
4) For voltage level $V_{an} = -V_{dc}/4$, turn on one upper switch $S_4$ and three lower switches $S_1$' – $S_3$'.
5) For voltage level $V_{an} = -V_{dc}/2$, turn on all lower switches $S_1$'–$S_4$'.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are ($S_1$, S2'), ($S_2$, $S_2$'), ($S_3$, $S_3$'), and ($S_4$, $S_4$')

### *D. Advantages of Diode Clamped Multi Level Inverter*

1) All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive.
2) The capacitors can be pre-charged as a group.
3) Efficiency is high for fundamental frequency switching.

### *E. Disadvantages of Diode Clamped Multi Level Inverter*

1) Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
2) The number of clamping diodes required is quadratic ally related to the number of levels, which can be cumbersome for units with a high number of levels

(Our work is concerned with diode clamped multilevel inverter.)

## II. CONTROL STRATEGIES OF MULTILEVEL INVERTER

The modulation methods used in multilevel inverters can be classified according to switching frequency. Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Another interesting alternative is the SVM strategy, which has been used in three-level inverters.

Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform. Representatives of this family are the multilevel selective harmonic elimination and the space-vector control (SVC).

1) Sinusoidal Pulse Width Modulation
2) Space Vector Modulation
3) Selective Harmonic Eliminated Pulse Width Modulation

(Here we just focus on Sinusoidal Pulse Width Modulation)

*Sinusoidal Pulse Width Modulation (SPWM)*

The control principle of SPWM is to use several triangular carrier signals keeping only one modulating sinusoidal signal. For A three level inverter two triangular carrier wave are needed (if m level inverter is employed (m-1) carrier will be needed).

The carrier has the same frequency fc for same peak to peak amplitude Ac. The zero reference is placed in the middle of carrier set. The modulating signal is a sinusoid of frequency fm and the amplitude Am. At every instant, each carrier is compared with modulating signal. Each comparison switches the switch "ON" if the modulating signal is greater than the triangular carrier wave assigned to that switch.

The actual driving signal for the power device can be derived from the result of the modulating – carrier comparison by means of logic circuit

## III. SIMULATION

### *A. Control Circuit of 3 Level Diode Clamped Inverter:*

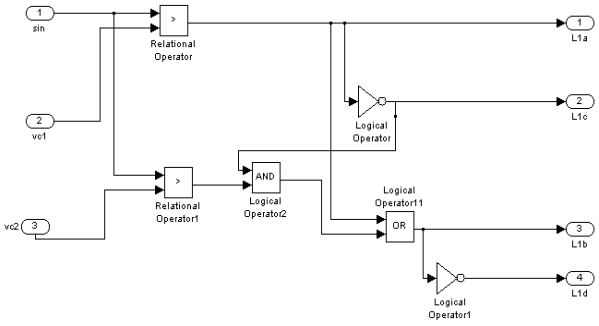



Fig. 4: Control circuit of 3 Level diode clamped inverter

In this, we have shown simulation results of 3-level and 5-level diode clamped multilevel inverter. In both 3 levels& 5 levels the control strategy used is level shifting SPWM.

As shown in fig 4 Control circuit is Design. Where, sin is the sinusoidal wave i.e. modulating wave, vc1 and vc2 are the triangular carrier wave 1 and 2 respectively, L1a, L1b, L1c and L1d are the pulses provided to the MOSFETs the pulses provided to the MOSFETs. Similarly all three phases are supplied with the pulses.

Here in this circuit the reference wave i.e. the sine wave and the two modulating waves that are triangular wave are compared with the above given logic circuit. Comparison logic is given in Table 1

*B. Power Circuit Of 3 Level Diode Clamped Inverter:*

The operating states of the switches are given in the Table 3.2.

*C. Simulation Results for 3-Level Diode Clamped Inverter:*

Here all the sine waves are compared with the carrier wave in order to get output for a three phase 3- level inverter.

Here the first sine wave is compared with the both triangular wave and the output pulses are obtained when sine wave is greater than the triangular wave. This will form the input for the 1st phase leg of the power circuit.

A simulation result for each phases are depicted as shown in fig 5 to fig 3.8

| | | Switching states | | | |
|---|---|---|---|---|---|
| | | M1_ out | M1_ in | M4_ in | M4_ Out |
| -Vdc/2 | 0 | 0 | 0 | 0 | 1 |
| 0 | Vdc/2 | 0 | 1 | 1 | 0 |
| Vdc/2 | Vdc | 1 | 1 | 1 | 0 |

Table. 1: Switches Status for A-phase

| Condition | Switches Status for A-phase | Output voltage |
|---|---|---|
| Vr>(Vt1,Vt2) | MOSFET_1OUT=ON, MOSFET_1IN=ON MOSFET_4IN=OFF, MOSFET_4OUT=OFF | Vdc/2 |
| Vt1>Vr>Vt2 | MOSFET_1OUT=OFF, MOSFET_1IN=ON MOSFET_4IN=ON, MOSFET_4OUT=OFF | 0 |
| Vr<(Vt1,Vt2) | MOSFET_1OUT=OFF, MOSFET_1IN=OFF MOSFET_4IN=ON, MOSFET_4OUT=ON | -Vdc/2 |

Table. 2: Switch states

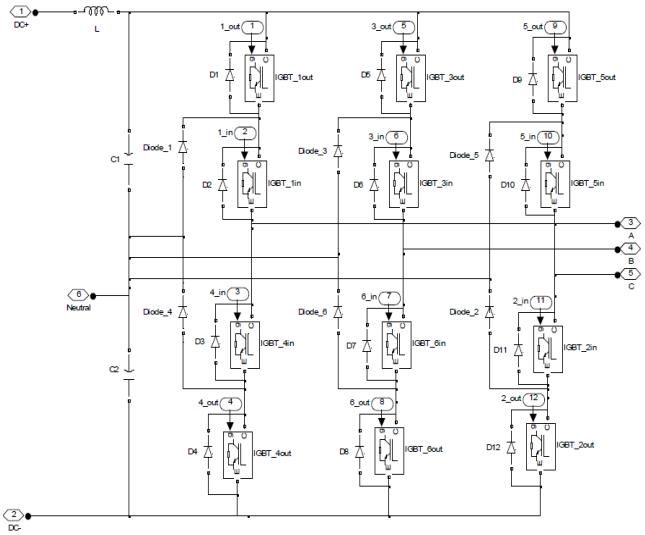


Fig. 5: Power circuit of 3 level diode clamped inverter

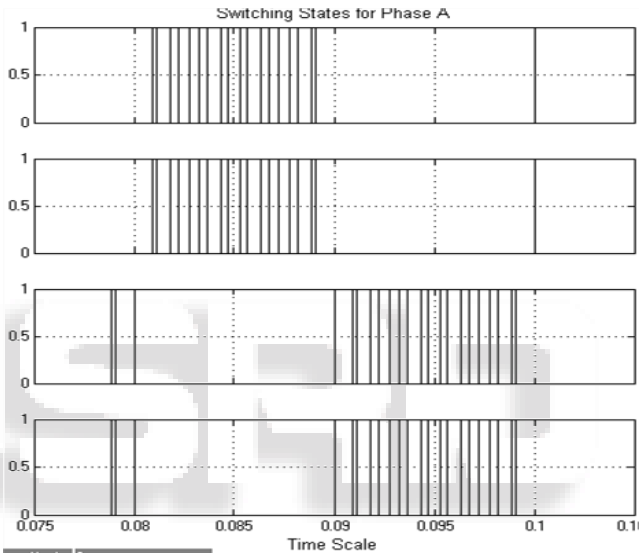



Fig. 6: Input for the 1st phase leg of the power circuit.

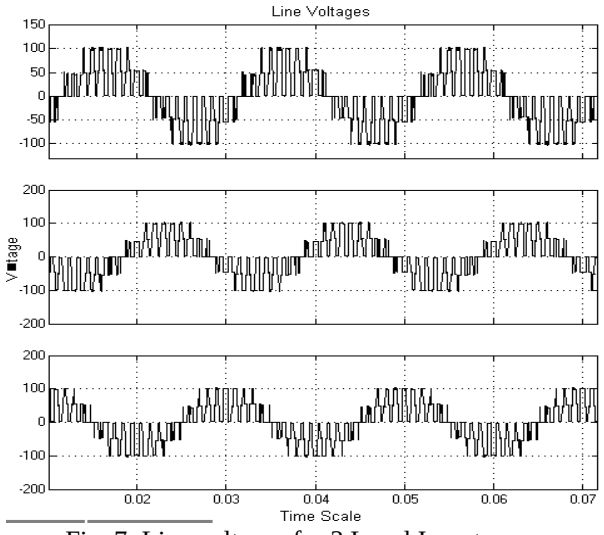



Fig. 7: Line voltages for 3 Level Inverter.

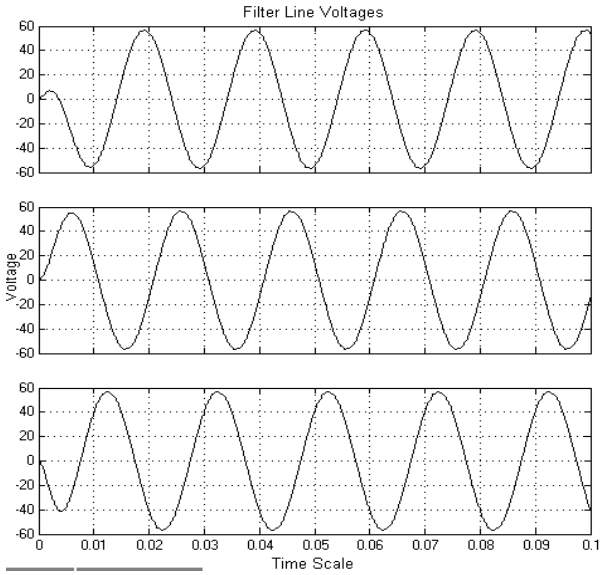



Fig. 8: Filter Line voltage for 3 Level inverter

*D. Simulation Results for 5-Level Diode Clamped Inverter:*

In this configuration four triangular waves i.e. carrier wave which are level disposed and one sine wave i.e. reference wave are compared and the output is fed to the power circuit. The simulation Results for 5 level inverter

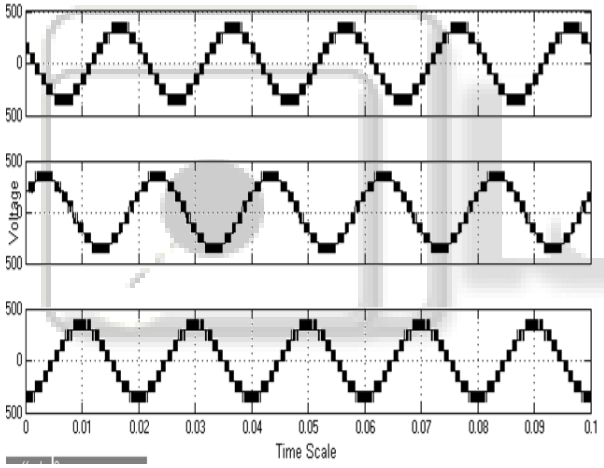



Fig. 9: Line Voltage of 5 Level inverter.

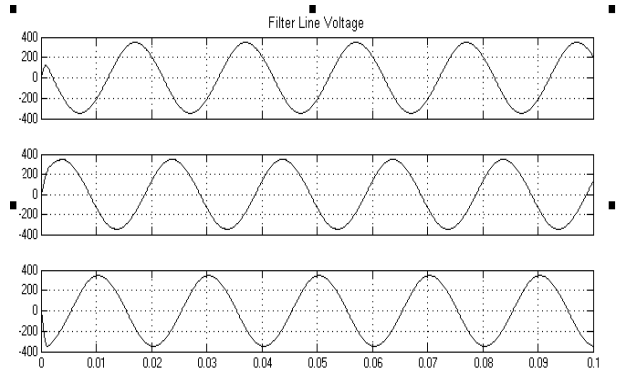



Fig. 10: Filter Line voltages for 5 Level Inverter.

## IV. FFT Analysis Of 3-Levels And 5-Levels MLI

To understand the 3levels and 5levels inverter Topology, here we perform FFT analysis for their particular Line-Line voltages as shown in fig

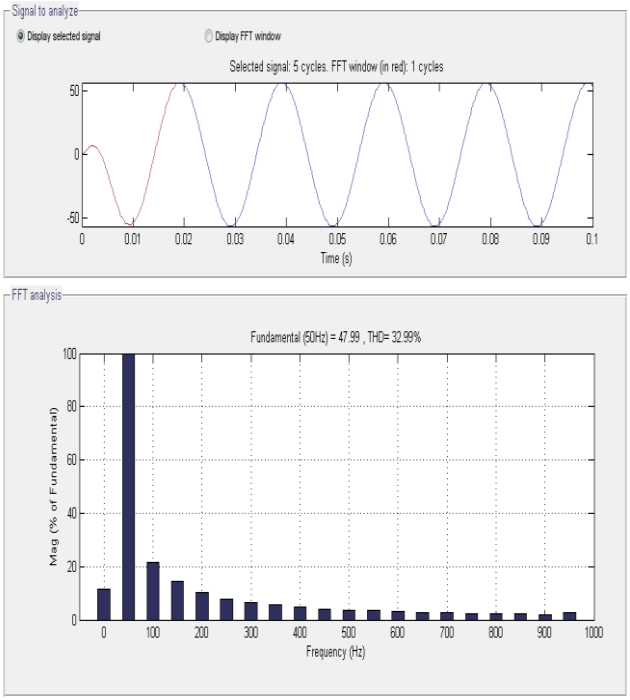
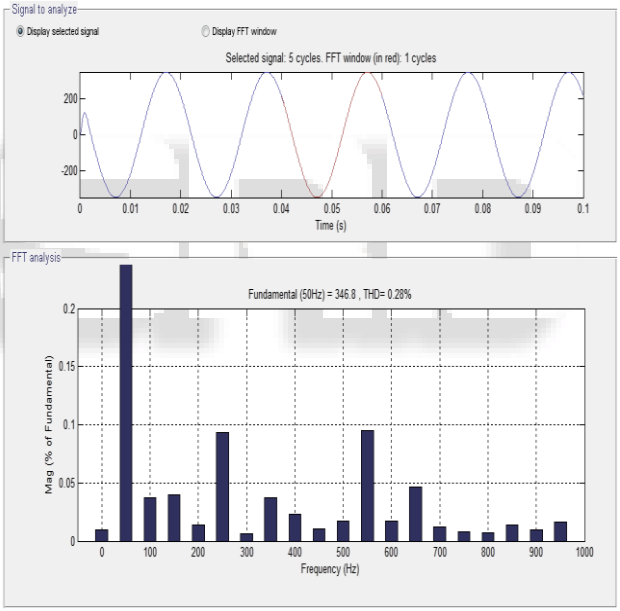



Fig. 11: FFT analysis results for 3levels inverter




Fi. 12: FFT analysis results for 5levels inverter

From the above result, we can analyse that for 3 levels and 5 levels inverter value of the THD is 32.99% and 0.28% respectively. That means it's always good to be having more no of levels as possible.

## V. Conclusion

It can be concluded that the simulation of 3-levels and 5-levels diode clamped inverters implementation are done similarly.

Also with five level simulation of diode clamped inverter it is known that more the levels of inverter, less distortion in the output waveform is obtained as we have seen in FFT analysis.

REFERENCES

[1] IEEE Transactions on Industrial Electronics, Rodriguez, J. Jih-Sheng Lai Fang Zhengpeng "Multilevel Inverters: A Survey Of Topologies, Controls, And Applications", Vol.49, No.4, August 2002
[2] IEEE Transactions on Power Electronics, Falcondes Jose Mendes De Seixas and Ivo Barbi, "A 12 KW Three-Phase Low THD Rectifier with High-Frequency Isolation and Regulated DC Output", Vol. 19, No. 2, March 2004, Pg No. 371 to 377.
[3] IEEE Transactions On Power Electronics Conference (IPEC), 2010 International Peng, F.Z., Wei Qian, Dong Cao, "Recent Advances In Multilevel Converter/Inverter Topologies And Applications" ,June 2010, Pg No. 492 - 501
[4] Rodrigues, T.S. Lai, F.Z.Peng, "Multilevel Inverter: Survey Of Topologies Control & Application", Aug-2002
[5] R.H.Baker&L.H.Bannister, "Electrical Power Converter", Feb-1975
[6] P.W.Hammond, "Four Quadrants AC-AC Drive & Method", Dec-2000
[7] I.Z.Peng, J.S.Lai, J.W.Mckeerer, "A Multilevel Voltage-Source Inverter", Sept-1996
[8] M.D.Manjrekar, "H Hybrids Inverter Topology For Drive Application", 1998
[9] Http://Www.Affordable-Solar.Com/Inverter.How.To.Htm
[10] Http://En.Wikipedia.Org/Wiki/Electromagnetic_Interference
[11] Http://Www.Wsicorporate.Com/Article/Multilevel_Inverter_Wiki