

CNTFET Modeling and Performance Analysis of Device Characteristics

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Abstract— Evolution of carbon nanotube based transistors is playing a vital role in today's shrinking technology and offers various advantages such as high channel mobility and improved gate capacitance against gate voltage. These devices have highly favorable characteristics in submicron regime in comparison with conventional MOSFETs and yields higher performance when considered for SoC design. This paper focuses on study of CNTFET transistors and examines the performance of CNTFET characteristics with respect to variation in tube length and chirality.

Key words: Carbon nano tube CNT; CNTFETs; MOSFETs; chiral

I. INTRODUCTION

As the MOSFETs are reaching their limitations with present day feature size of transistors, the semiconductor industry is looking for technologies that are least affected due to short channel effects. This directs the research towards nanoscale devices such as CNTFETs, Finfets; Nanowire FETs etc., such that there is need to exploit their properties when used for circuit design of sub -10nm regime.

Nano science research focuses primarily on the search for new physical concepts and on creating the technology necessary for the development of nano devices. However, research in nano electronic circuits (the integration of nano devices in circuits or systems), in the context of leading-edge technologies to realize data processing, memorization and communication functions, is somewhat under-represented. It is necessary to propose new computing or memory circuit structures based on nano devices and at quantifying their respective performance with respect to CMOS or SOI based circuits (in terms of integration density, speed, power and reliability) is the need of the hour[1]

The evolution of research has led us to promising materials such as Carbon nanotubes having a diameter ranging from 1 to 3 nm and the length can be up to several micrometers, they can be extensively used for interconnections because of their higher carbon-carbon bond strength and scalable feature. CNTs can be exploited to build both low-resistance high-strength interconnections and highly scalable low-power carbon nanotube field-effect transistors (CNTFET) and single electron tunneling transistors.

Presently, many research teams carryout studies about CNTFET devices and their logic applications all over the world, both in industrial laboratories (IBM, Intel, Infineon etc. and in universities like Purdue and Stanford, One of the basic ideas is to replace the silicon MOSFETs with CNTFETs to overcome all the limitations of silicon MOSFETs. However, the design of circuits based on such devices requires available device models, compatible with up-to-date design flows [2].

This paper in section II first describes the CNT physical properties and 3D modeling of the same; it also reviews the current device physics with respect to CNTs and

in section III various types of CNTFETs are discussed, in section IV the simulation results are presented and section V ends with conclusion of the work carried out.

II. STRUCTURE OF CARBON NANO TUBE

A Graphene sheet is rolled to form a carbon nanotube as depicted in fig1.

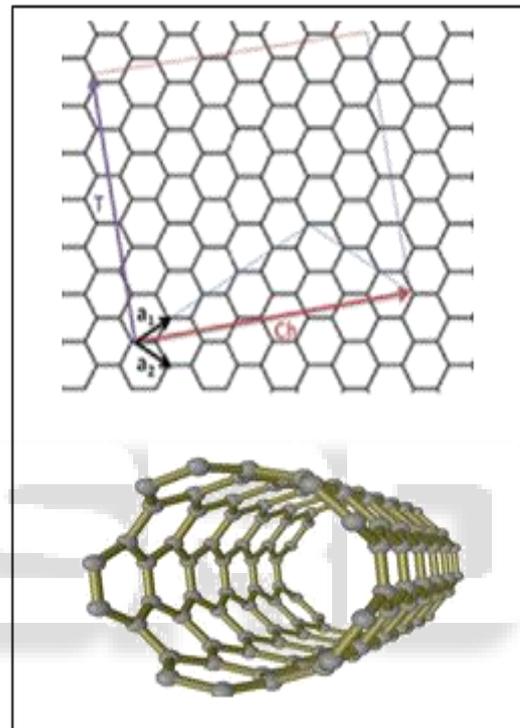


Fig. 1: Graphene sheet rolled to form a carbon nanotube[6]

The diameter of the tube is obtained by the chiral vector (Ch); $Ch = na_1 + ma_2$. Where (n, m) represents the chirality of the carbon nanotube.

The desired diameter of CNT is obtained by by changing the chirality while keeping the channel length constant. If (n, m) is the chirality of a CNT, the diameter of the CNT is given as:

$$d = \frac{a \sqrt{(n^2 + m^2 + nm)}}{\pi}$$

Where 'a' is the length of the graphene basis vector.

T is the vector perpendicular to Ch. To form a nanotube, the graphene sheet should be rolled around an axis parallel to T. If $m=n$ it is known as armchair nanotube and if either m or n is equal to zero then the tube is known as zigzag nanotube

The CNT used can be either single walled or multi walled as shown below

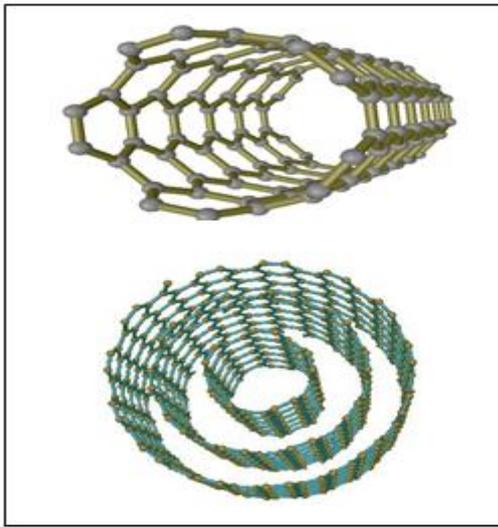


Fig. 2: 3D modeling of Single and Multiwalled CNTs

Single-wall (SW) carbon nanotubes (CNTs), used as transistor channels, are sheets of graphene rolled into tubes. CNT properties are strongly dependent on their chirality (way the sheet is rolled up) and diameter. In function of the chiral vector, CNTs may be metallic or semi-conducting. Semi-conducting nanotubes are direct band-gap semi-conducting with band-gap $E_G \approx 0.9/d$ (eV), where d is the nanotube diameter. Low-field transport is near-ballistic with mobility as high as $\sim 100,000 \text{ cm}^2/\text{Vs}$ [4]

In coaxial gate the gate capacitance is given by

$$C_G = \frac{2\pi\epsilon_0\epsilon_r L}{\ln[2(t_{ins} + r) / r]}$$

Where r is the radius of nano tube, t_{ins} is the oxide thickness
 L is the length of gate.

In case of planar gate the expression for gate capacitance is as depicted below [2]

$$C_G = \frac{2\pi\epsilon_0\epsilon_r L}{\cosh^{-1}(t_{ins} / r)}$$

Figure 3 depicts the band structure of carbon nano tube with CC bond length of 0.142 for bonding and anti-bonding data

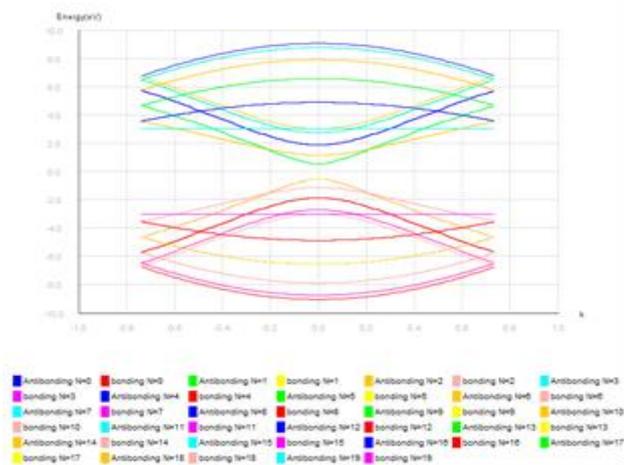


Fig. 3: band structure of carbon nano tube with CC bond length of 0.142

III. TYPES OF CNTFETS

There are three types of CNTFETs fabricated so far.

- Schottky-barrier (SB) CNTFET (fig.4a),
- Partially-gated (PG) CNTFET (fig.4b) and
- Doped-S/D CNTFET (fig.4c)

In SB CNTFETs, the gate modulates the tunneling transmission through a SB between the source metal and the nanotube channel. SB-CNTFETs exhibit strong ambipolar characteristics, which limit the use of these transistors in conventional CMOS-like logic families

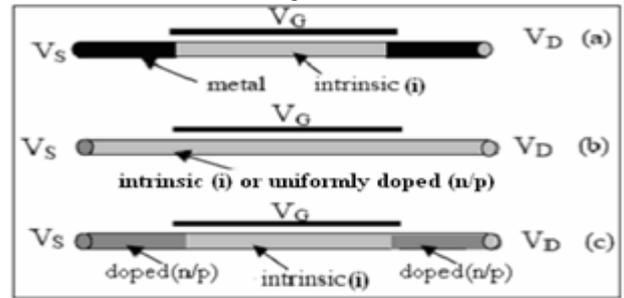


Fig. 4a, 4b and 4c: Types of CNTFETS [5]

In PG CNTFETs they have uniformly doped ohmic contacts at their ends as shown in fig 4b; the doping can be of n type or p type. The gate locally depletes charge carriers to turn on/off the device

Doped-S/D CNTFETs presented in Fig. 4(c) are composed of two un-gated portions that are heavily or lightly n/p doped.

The ON current is limited by the amount of charge that can be induced in the channel by the gate and not by the doping in the source. They operate in a pure p- or n-type enhancement mode or in a depletion mode, based on the principle of barrier height modulation when applying a gate potential.

The doped S/D CNTFETs are promising because of following reasons

- They only show unipolar characteristics,
- The absence of SB reduces the Off leakage current;
- They are more scalable compared to their SB counterparts;
- In the ON-state, the source-to-channel junction has a significantly higher ON current.

However, controlled doping is very difficult and ion implantation techniques must be avoided because the ions may replace carbon atoms and destroy the desired nanotube properties. [4]

Depending on the type of Geometry we classify the CNTFETs as

- Planar CNTFETS
- Coaxial gated CNTFETs or cylindrical CNTFETs

A. Planar CNTFETS:

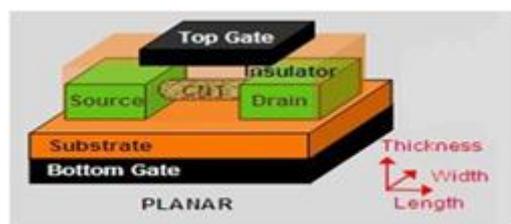


Fig 5a .Planar CNTFET

Planar CNTFETs constitute the majority of devices fabricated to date, mostly due to their relative simplicity and moderate compatibility with existing manufacturing technologies. The nanotube and the metallic source-drain contacts are arranged on an insulated substrate, with either the nanotube being draped over the pre-patterned contacts, or with the contacts being patterned over the nanotube. In the latter case, the nanotubes are usually dispersed in a solution and transferred to a substrate containing pre-arranged electrodes.

B. Coaxially gated CNTFETs:

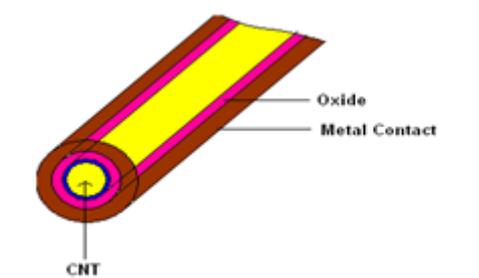


Fig. 5b: coaxially gated CNTFET [5]

This consists of a single walled CNT with a coaxial gate. In this device the coaxially placed CNT plays the role of channel which is surrounded by a cylindrical gate separated by a layer of oxide.

IV. SIMULATION RESULTS

A. Drain Current V/S Voltage:

The simulation work is carried out using nano hub tools by varying the CNT length keeping the chiral vector values constant and all other operating conditions are kept same;

The $I_d - V_d$ curves are obtained for different CNT lengths and performance is analyzed. Similarly the characteristics are obtained for different chiral vectors such that the diameter of the CNT changes.

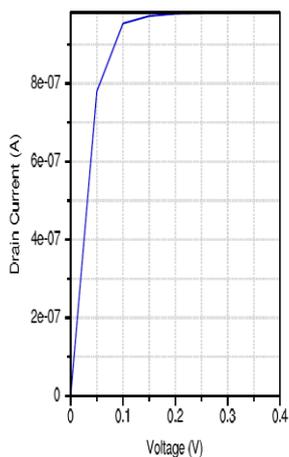


Fig. 6(a)

Fig. 6a: Depicts the Voltage V/s Drain current plot of CNTFET with channel length=10nm and Chiral vector(m=0,n=13)

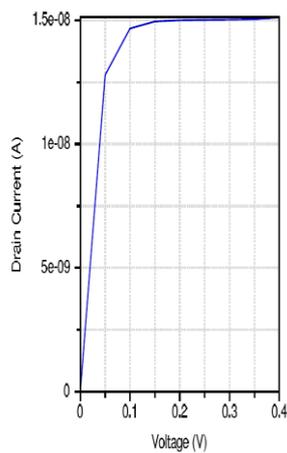


Fig. 6(b)

Fig. 6b: Depicts the Voltage V/s Drain current plot of CNTFET with channel length=5 nm and Chiral vector(m=0,n=13)

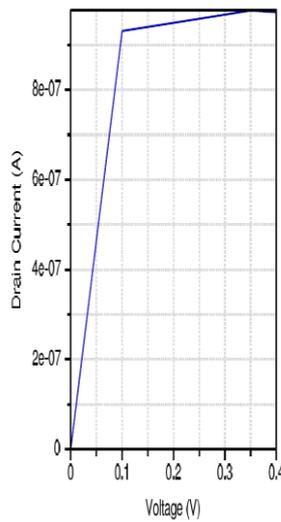


Fig 6c

Fig. 6c: Depicts the Voltage V/s Drain current plot of CNTFET with channel length=15nm and Chiral vector (m=0,n=10)

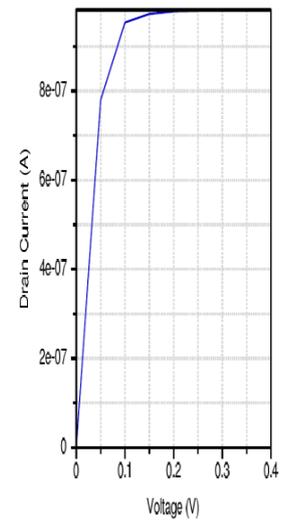


Fig.6d

Fig. 6d: Depicts the Voltage V/s Drain current plot of CNTFET with channel length=10 nm and Chiral vector (m=0,n=10)

The above plots of voltage v/s drain current are obtained by keeping the ambient temperature at 300Kelvin and gate and drain voltages are 0.4 volts with voltage applied in steps of 0.05volts.

The other device parameters such as source drain thickness, source drain width are fixed at 7nm and 15nm respectively and gate thickness is fixed at 5nm. Device width is fixed at 20nm. The source contact work function difference of carbon nanotube is fixed at 0.41 eV throughout the simulation

By fixing the channel chirality constant we make the diameter of the tube constant, with constant tube diameter if we vary the channel length it is evident from the above plots that as the channel length reduces, we have higher value of drain current for the CNTFETs and also Saturation current is more for tubes with lesser diameter.

B. Density V/S Distance:

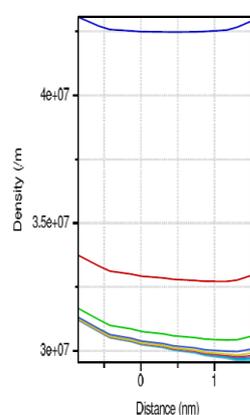


Fig.7(a)

Fig. 7a: Depicts the density v/s distance plot of CNTFET with channel length=1nm and Chiral vector (m=0,n=10)

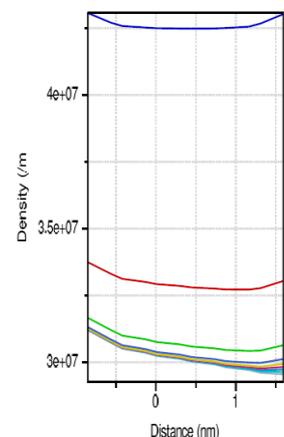


Fig. 7(b)

Fig. 7b: Depicts the density v/s distance plot of CNTFET with channel length=3 nm and Chiral vector (m=0,n=10)

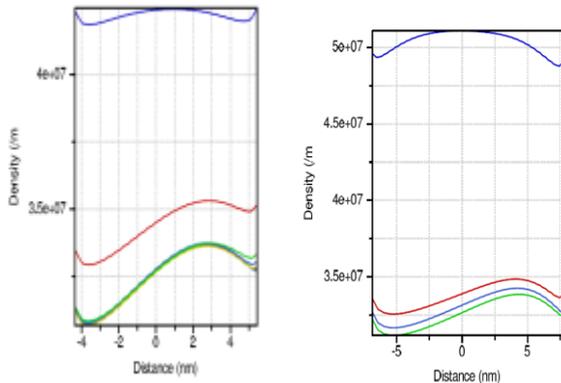


Fig. 7(c)

Fig. 7(d)

Fig. 7c: Depicts the density v/s distance plot of CNTFET with channel length=10nm and Chiral vector (m=0,n=10)

Fig. 7d: Depicts the density v/s distance plot of CNTFET with channel length=15 nm and Chiral vector (m=0,n=10)

As depicted in the fig 7 by keeping the chirality constant if we increase the channel length the carrier density will increase, also the level of on current has increased with increase in diameter, using the larger diameter reduces the band gap and hence the on current increases, but a necessary tradeoff has to be made for choosing the channel diameter as the on current increase the leakage current will also increase, hence this issue need to be addressed by selection of proper chiral ratio such that the leakage currents should not have a drastic increase. This parameter is important will allow us while designing logic circuits based on CNTFETs

V. CONCLUSION

This paper provides an overview of how carbon nano tubes are formed using graphene ribbons and also presents a 3D view of single walled and Multiwall CNTs. It also discusses briefly about the different types of CNTFETs. Planar CNTFETs are considered for simulation and some important aspects of the behavior of CNTFETS under parameter variation are investigated. An interesting conclusion is that the carbon nano tube diameter influences both the current level and the carrier density of the device. This characteristic plots obtained in simulation greatly infers the behavior of the device under variation of channel length and diameter, which must be carefully taken into account while designing robust logic circuits based on CNTFETs.

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