Design and Implementation of Sense Amplifier based Flip Flop for High Performance in CMOS 45nm Technology Parameter

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Abstract---**T**his paper will demonstrate the sense amplifier based flip flop design using static or conventional CMOS and NIKOLIC latch based topologies. Implementation is done using BPTM 45nm deep submicron technology parameter in LT spice IV. Sense amplifier plays important role in memory read and write operation which will reduce the power consumption and propagation delay. I have designed D flip flop with both logic topologies and results found a lesser power consumption and propagation delay in NIKOLIC architecture compared to conventional sense amplifier based flip flop.

Key words: CMOS, BPTM, CSAFF, NIKOLIC.

I. INTRODUCTION

When reading a memory cell, bit lines are initially precharged. In the memory operation, one of the bit lines goes down and one remain charged. The pulling down of the bit line is very slow because the discharging through MOS is low and the capacitance of the bit line is very high. So, delay will increases in reading the data of the memory. Sense amplifiers are used to detect small variation on bit lines and produce full swing.

A square memory is designed, for selecting the proper row for reading or writing the data a row decoder is used. Column decoder is used to select a proper memory cell. Sense amplifier is connected with the memory cell so that it can detect and amplify the signal. A proper sense amplifier is used in design the memory.

In certain memory structure, amplification is required for proper functionality since the typical circuit swing is limited. In other memories, it allows resolving data with small bit line swings, enabling reduced power dissipation and delay. The amplifier detects and amplifies small transition on the bit line to large signal output swings, due to which a small swing input is used and the delay will reduce. Reducing the signal swing on bit lines can eliminate a substantial part of power dissipation related to charging and discharging the bit lines.

The memory elements in these circuits are called flip-flops. A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the stored bit. Binary information can enter a flip-flop in a variety of ways and gives rise to different types of flip-flops. There are various types of like R-S, D, T or J-K flip flops.

II. CONVENTIONAL SAFF

SAFF incorporates a pre-charged sense amplifier in the first stage to generate a negative pulse, and a Set-Reset (SR) latch in the second stage to capture the pulse and hold the results. Since my proposed design is based on SAFF, let us first consider the operation of sense-amplifier flip-flop in more detail.

The schematic of sense-amplifier flip-flop is shown in Fig.2. Simulation result is shown in Fig.3. The circuit works as follows: when the clock is in precharge mode, the master stage nodes (S and R) are both charged to VDD using two PMOS transistors (MP1and MP2). When the rising edge of the clock arrives, S or R is discharged to ground depending on the value of input (D). In the case when D is high, three stacked NMOS transistors discharge node S to ground that causes output (Q) to charge to "1". Due to the cross-coupled inverters, R remains high. Note that SAFF comes with delay penalty. This is due to two reasons the use of three stacked NMOS transistors and the low speed of the static output latch. In terms of power, SAFF outperforms its counterparts due to stacking effect and minimum sized design.

III. NIKOLIC LATCH

The circuit employs two inverters to evaluate the signals. The four signals and are used to drive four devices N1, N2, P1, and P2 which are devoted to switching and output nodes. The remaining eight devices N3–N6 and P3–P6 are minimum sized and hold the latch state for, providing a fully static operation with a ratioless sizing.

If S and R are high, the latch is in the hold state. In fact, and are both low and the devices N1, N2, P1, and P2 are OFF. The devices N3, N5, P3and P5 are ON, and, consequently, N4, N6, P4, and P6 hold the latch state. Let us now assume that the flip-flop master stage switches, driving low. Device P1 is turned on, and node is quickly driven high. Note that this transition is ratioless and without crow-bar current since N1 is OFF, and also shuts off device N3 which opens the remaining pull-down path for node. Moreover, signal goes high, and N2 turns on driving low. This second transition is also ratioless and without crow-bar current owing to the P5 device. Hence, in addition to the sense-amplifier delay, I have one-gate delay for the low-to-high output transition and a two-gate delay for the high-to-low output transition. The schematic of NIKOLIC sense-amplifier flip-flop is shown in Fig.5. Simulation result is shown in Fig.6.

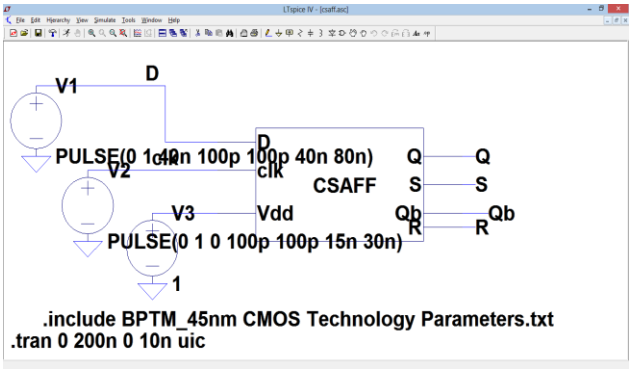

Fig.1: Block diagram of CSAFF.

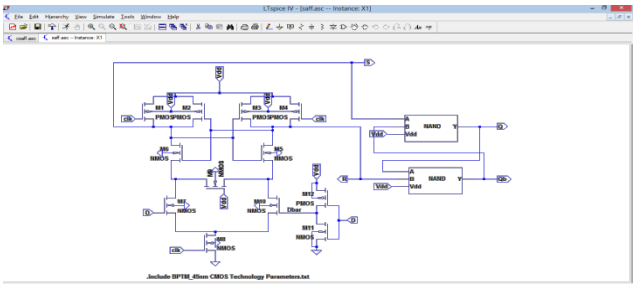

Fig. 2: Schematic of CSAFF.

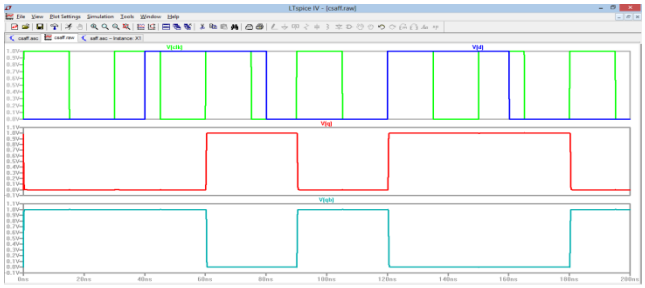

Fig. 3: Simulation result of CSAFF.

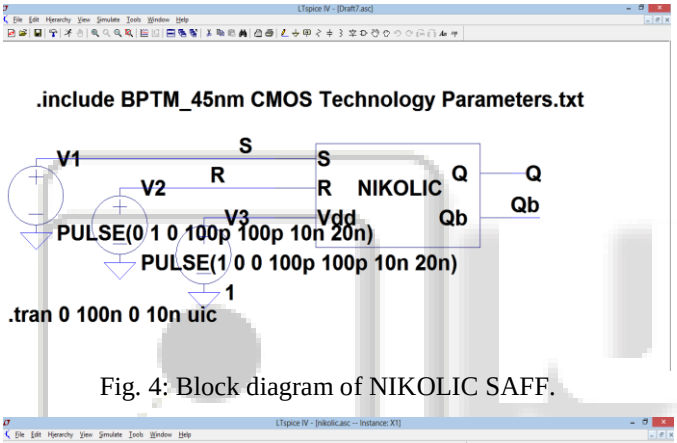

Fig. 4: Block diagram of NIKOLIC SAFF.

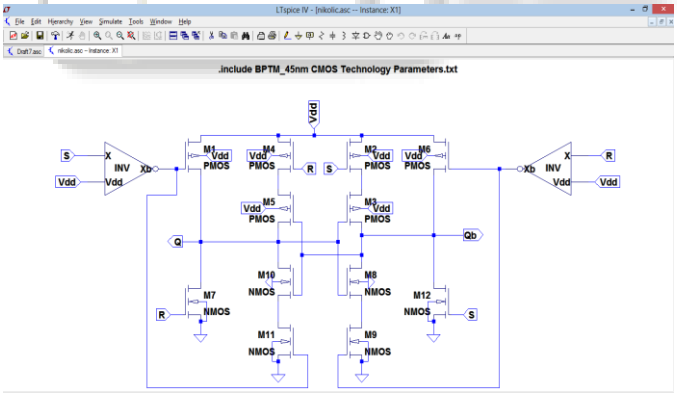

Fig. 5: Schematic of NIKOLIC SAFF.

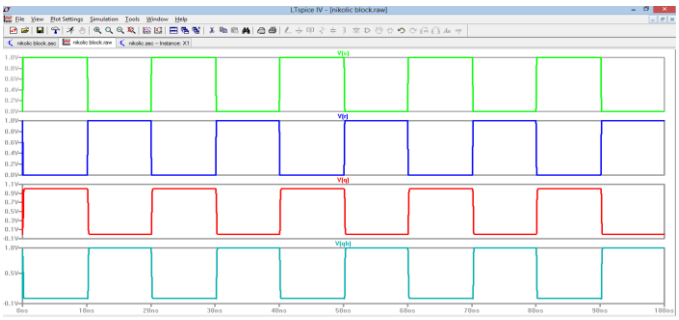

Fig .6: Simulation Result of NIKOLIC SAFF.

IV. Comparative Analysis

As described in the previous session that conventional sense amplifier based flip flop is triggered at only positive charge edge of the clock signal, so when input signal rise or drop to zero than also latch has to wait for the positive edge of the clock signal until this there is no change in the output Q as shown in figure 3.

This problem can be overcome by using the design given by NIKOLIC latch will reduce the use of the clock signal so as its input changes state than output also changes instantly so it reduces the output sensing capability of the latch, with this as I can see that average power consumption, rise time, fall time and power delay product (PDP) is less as compared to the conventional sense amplifier based flip flop.

Parameters	Average Power Dissipation (uW)	Rise Time (pS)	Fall Time (pS)	PDP (fJ)
CSAFF	2.372	244.746	220.379	474.4
NIKOLIC	1.4461	81.7955	89.1892	144.61

Table. 1: Comparative analysis of CSAFF and NIKOLIC SAFF

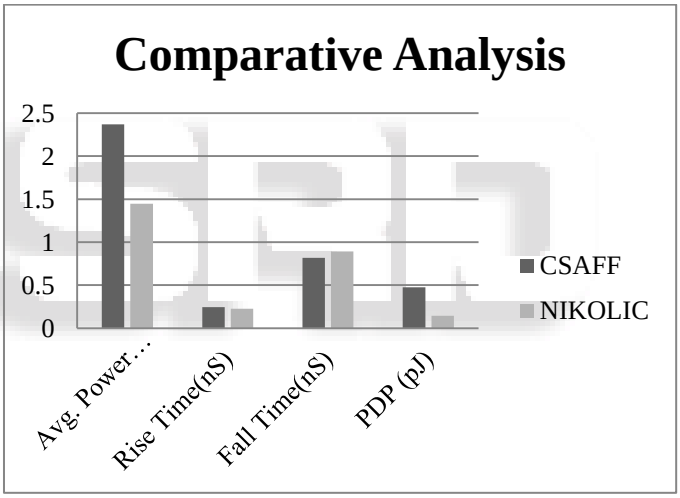

Fig. 7: Graphical representation of comparative analysis.

V. Conclusion

A sense amplifier is the most widely used device in the memory systems for data sensing and storing purposes. there are different variety of sense amplifier based flip flop are designed and used in real time memory, but most demanding are the least propagation delay and the power consumption are mostly required. here I have designed and implemented two architecture of flip flop called conventional sense amplifier flip flop(CSAFF) and NIKOLIC latch based flip flop, by comparing performance parameter I can conclude that NIKOLIC latch had a better and least power consumption of 1.4461uW and rise time of 81.79pS and fall time of 89.1892pS at supply voltage Vdd of 1V.

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