An Overview of Advance Microcontroller Bus Architecture Related on AHB Bridge

Ayushi Shah[1]
[1]P.G Student
[1]Department of Electronics Engineering
[1]Gujarat Technological University, Ahmedabad, Gujarat, India

Abstract— In this paper I introduced on chip communication standard called AMBA AHB. The AMBA AHB is for high-performance, high clock frequency system modules. AHB support the efficient connection between embedded processor, on chip memory and of chip external interface or bridge with low power peripheral Macrocell functions. AMBA AHB is basically single layer bus. It includes all AMBA AHB signal or specification which provides an infrastructure for diagnostic access and Macrocell test.

Key words: AMBA, AHB, ASB, APB, Bridge, Compression of buse

I. INTRODUCTION

The advance microcontroller bus architecture (AMBA) is an open standard, on chip communication standard for designing high performance embedded microcontrollers. It facilitates development of multiprocessor designs with large numbers of controllers and peripherals. Today, AMBA is widely used on a range of ASIC and SoC parts including applications processors used in modern portable mobile devices. AMBA was introduced by ARM in 1996. The first AMBA buses were Advanced System Bus (ASB) and Advanced Peripheral Bus (APB). The second version is, AMBA 2, ARM added AMBA Advance High-performance Bus (AHB) that is a single clock-edge protocol. In 2003, ARM introduced the third generation, AMBA 3, including Advance eXtensible Interface (AXI) to reach even higher performance interconnects and the Advanced Trace Bus (ATB) as part of the Core Sight on-chip debug and trace solution. In 2010 the AMBA 4 specifications were introduced starting with AMBA 4 AXI4, then in 2011 ARM added AXI Coherency Extensions (ACE) with additional signaling and wide range. In 2013 the AMBA 5 CHI (Coherent Hub Interface) specification was introduced, with a re-designed high-speed transport layer and features designed to reduce congestion.

II. AN OVERVIEW OF AMBA BUSES

The advance micro controller bus architecture (AMBA) is an open standard, on chip communication standard for designing high performance embedded microcontrollers. It facilitates development of multi-processor designs with large numbers of controllers and peripherals. Today, AMBA is widely used on a range of ASIC and SoC parts including applications processors used in modern portable mobile devices.

AMBA specifications [1] are derived to satisfy following four different requirements:

(1) To facilitate the run-first-time development of Embedded Microcontroller products with one or more CPUS or signal processors.
(2) To be technology independent and ensure that highly reusable peripheral and system microcell can be migrated across a diverse range of IC processors and be appropriate for full custom, standard cells, and gate array technologies.
(3) To encourage modular system design to improve processor independence, providing a development road-map for advanced cached CPU cores and the development of peripheral libraries.
(4) To minimize the silicon infrastructure required supporting efficient on-chip and off-chip communication for both operation and manufacturing test.

Three different buses are defines within AMBA specification.

A. Advanced High Performance bus (AHB):

The AMBA AHB is high performance, high clock frequency system module. The AHB act as a high performance system bus. It supports the efficient connection between processors, on-chip memories and off- chip external memory interface.

B. Advanced Peripheral Bus (APB):

The AMBA APB is for low-power peripherals. It is designed for low bandwidth control access. AMBA APB is optimized for minimal power consumption and reduced interface complexity to support peripheral functions. APB can be used in conjunction with either version of the system bus. It is usually used in peripheral devices with low bandwidth.

C. Advanced System Bus(ASB):

The AMBA ASB is for high-performance system modules.
It is an alternative system bus suitable for use where the high-performance features of AHB are not required. ASB also supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral macrocell functions.

III. ABOUT AMBA AHB

AHB is a new generation of AMBA bus which is designed to address the requirements of high-performance and high clock frequency synthesizable designs. High performance and high clock frequency include:

– burst transfers
– single cycle bus master handover
– split transactions
– Address Decoding.
– non-tristate implementation
– single clock edge operation
– SEQ, NONSEQ, IDLE, BUSY transfer types.
– wider data bus configurations (64/128 bits).

A. AMBA AHB Based Microctroller;

An AMBA-based microcontroller consists of a high-performance system bus, able to support the external memory bandwidth, on which the CPU and other *Direct Memory Access* (DMA) devices reside, plus a bridge to a narrower APB bus on which the lower bandwidth peripheral devices are located. Bridge located between system bus and peripheral bus. When the data is transferring from processor to peripheral device like UART, keyboard, peripheral I/O, timer, the bridge convert that transfer signal from one type to another for satisfying different performance and operation.

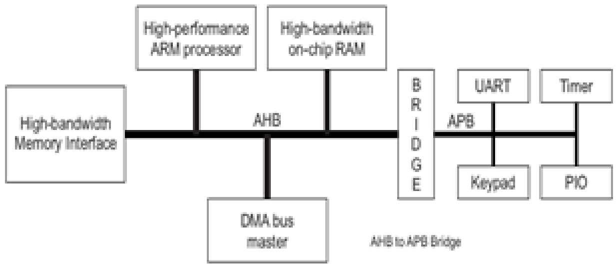

Fig. 1: A Typical AMBA AHB BASED System

B. AMBA AHB Components;

The AMBA AHB design contains the following components:

- AHB Master is able to initiate read and write operations. This is done by providing an address and control information. Only one bus master is allowed to actively use the bus at any one time. AHB support at most 16 masters on bus.
- AHB Slave responds to a read or write operation within a given address-space range. The bus slave signals back the response to the active master the success, failure or waiting of the data transfer.
- AHB Arbiter ensures that only one bus master at a time is allowed to initiate data transfers at any one time. An AHB would include only one arbiter.
- AHB Decoder is used to decode the address of each transfer given by the master and provide a select signal for the slave that is involved in the transfer. A single centralize decoder is used in all AHB implementations.

C. Bus Interconnection:

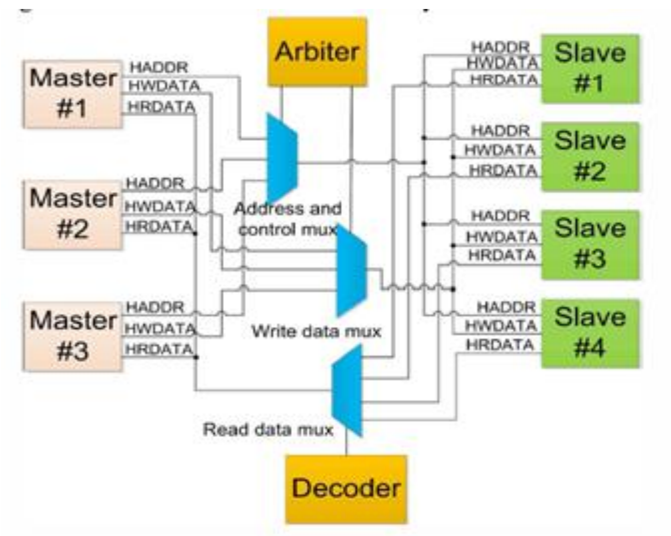

Fig. 2: Multiplexor interconnection

IV. PROPOSED DESIGN FOR BRIDGE

The ARM processor and AHB bus are more popular in SoC design. Bus has many advantages in high-performance devices but has limitations on interface with low bandwidth devices. So, bridge is necessary between them. AMBA AHB and ASB is high performance bus and have higher bandwidth. High bandwidth RAM, DMA bus controller, memory interface and high performance ARM processors which require high bandwidth are connected with AHB or ASB. Whereas APB is low bandwidth and low performance bus. Peripheral devices such as UART, Timer, and keypad require low bandwidth, so connects with APB. So bridge is required to connect AHB or ASB and APB.

AHB-to-APB Bridge interfaces AHB and APB. It is require to bridge communication gap between high bandwidth AHB and low bandwidth peripheral like serial, Ethernet devices on APB [2].

There are many differences between these two buses. AHB uses full duplex communication where as APB uses massive memory-I/O accesses. Unlike AHB, there is no pipelined structure in APB. Compared with AHB, APB has low bandwidth control accesses.

Looking at the features of AHB, it supports single edge clock protocol, split transaction, several bus masters, variable and large bus widths, burst transfer and non-tri state implementation.

If comparing usage, APB is simpler than AHB. APB is mainly proposed for connecting to simple low bandwidth peripherals. APB also can be optimized for reduce the interface complexity and power consumption.

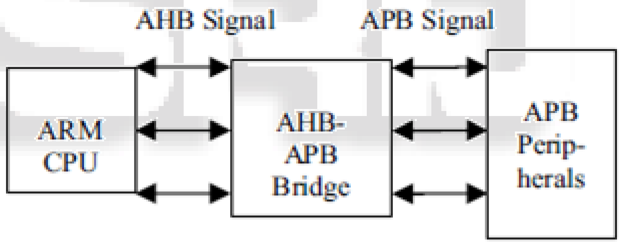

Fig. 3: Application Block Diagram of AHB2APB.

Figure 3, shows application block diagram for AHB2APB Bridge. The master is ARM CPU and slaves are APB peripherals. It is assumed that speed ratio of AHB2APB is 2:1 i.e. if AHB executes with clock frequency 200MHz, APB should be with 100MHz. So, Bridge is required for frequency and speed compensation between system and local bus.

Bridge provides latching of control, data and address signals for APB peripheral devices.

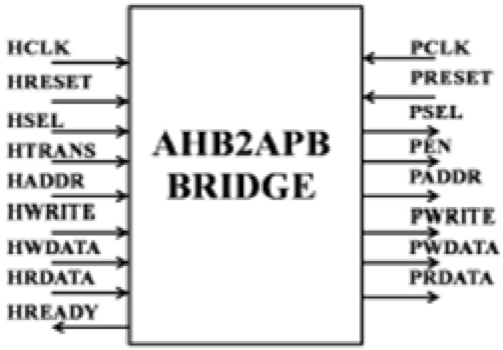

Fig. 4: Pin Details for AHB2APB Bridge

Bridge operates on CLOCK and RESET AHB. There is control transfer block between AHB response and APB access. Control transfer block is used to transfer AHB control signal to APB access with appropriate delay to map AHB pipelined protocol with two cycles APB protocol. Valid commands are forwarded to control transfer for action. For invalid commands, error message is produced and commands are not forwarded. APB access used to generate control signals for read/write cycles on APB.

V. COMPARISON OF AMBA BUSES

Table 1 shows the comparison between different AMBA buses.

Parameters	**AHB**	**ASB**	**APB**
Performance	High	High	Low power
Components	Master, slave, arbiter, decoder	Master, slave, arbiter, decoder	APB bridge and slave
Operation	Pipelined operation	Pipelined operation	Latched address and control operation
Multiple bus master	Yes	Yes	Simple interface
Split transaction	Yes	No	No
Burst transfers	Yes	Yes	Suitable for many peripherals

Table 1: Comparison of Buses

VI. CONCLUSION

This paper proposed an overview of widely used on-chip buses in SoC design and interface of IP Cores. We describe the methodology for designing of bus master bridges. Bridge is intended to make communication between two buses which have different functionality and characteristics. By using bridge, we can achieve error free communication between two different bus architectures.

REFERENCES

[1] ARM. “AMBA Specification (Rev. 2.0), 1999. Available [Online] at: http://www.arm.com/
[2] Vani R. M, Roopa M, “Design of AHB2APB Bridge for Different Phase and Frequency”, IJCEE, Vol. 3, No.2, April, 2011.
[3] Manu B.N, Prabhavathi P, “Design and Implementation of AMBA ASB APB Bridge”, IEEE, Taiwan, DEC.6-8, 2013.
[4] Priyanka Gandhani, Charu Patel “ Moving from AMBA AHB to AXI Bus in SoC Designs: A Comparative Study” Int. J Comp Sci. Emerging Tech Vol-2 No 4 ,pp.476-479 August, 2011
[5] Wang Zhonghai,Ye Yizheng,Wang Jinxing, and Yu Mingyan, “Design-ing AHB/PCI Bridge,”in Proceedings of 4th International Conference on ASIC, Oct 2001,pp.578-580.