

Low Power and High Speed CMOS Comparator for A/D Converter Applications - A Review

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Abstract—In high-speed high-resolution analog to digital converters, comparators have a key role in quality of performance. High power consumption is one of the drawbacks of these circuits which can be reduced by using suitable architectures. Many versions of comparator are proposed to achieve desirable output in sub-micron and deep sub-micron design technologies. The selection of particular topology is dependent upon the requirements and applications of the design. Low power and high speed circuit design has emerged as a principal theme in today's electronics industry. In this paper, a basic SA-ADC (successive approximation) is discussed as a proper choice for low power applications and comparison with other ADC architectures. Following with the study of design parameters of comparator, their architectures and its use in various applications.

Keywords: CMOS comparator, offset voltages, power consumption, SA-ADC, speed.

I. INTRODUCTION

The rapidly growing market of portable electronic systems such as wireless communication devices, consumer electronics or battery-powered medical devices increases the demand for developing low voltage and low-power circuit techniques and building blocks. One such application where low power, high resolution and high speed are required is analog-to-digital converters (ADCs) as a key components in mixed-signal integrated circuits. Recent ADC applications are used increasingly in digital data reading fields, such as hard disk drives, digital video discs and local area networks. High sampling speed is required in all of these applications, best solution for high speed, low latency operations is flash architecture but performance degrades as number of comparators increases. Alternative to this folding CMOS comparator which reduces number of comparators but performance degrades due to process variation. A novel circuit for low power, low cost, high speed CMOS ADC is general successive approximation ADC is presented where comparators plays a key role.

II. LITERATURE SURVEY

Behzad Razavi and Bruce A. Wooley et. al., This paper presented precision techniques for the design of BICMOS and CMOS fast comparators used in high-performance analog-to-digital converters employing parallel conversion stages with careful trade-offs among parameters such as speed, resolution, power dissipation, and input capacitance. A CMOS comparator utilizing new offset cancellation techniques which significantly relaxes the preamplifier gain requirements, allowing high speed and low power dissipation are also discussed [5].

Mehdi Banihashemi, Khayrollah Hadidi, and Abdollah Khoei et. al., gives the method which can

effectively reduces the power consumption of the comparator as well as offset voltage. In conventional comparators, during preamplification, latch is idle. In order to save the power consumption of the latch in this mode and use this power to increase the speed. This was done by using a gain stage as a preamplifier in the preamplification mode and as a latch in the latch mode [2].

Michel Rouger, Pierre Lutz et.al., designed Low-Power Auto-zeroed High-Speed latch Comparator. The offset compensated comparator architecture used in this work. The comparator uses both input offset storage and output offset storage which is among the best offset cancellation techniques. This allows eliminating the offset voltages of both the stages using only one-capacitor pairs and offset sampling phase [7].

Heung Jun Jeon et.al., presented a novel fully dynamic a latched comparator which shows lower offset voltage and higher load drivability compared to conventional dynamic latched comparators. In this novel design a CMOS comparator circuit with two additional inverters inserted between the input and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage is improved. The complementary version of the regenerative latch stage, which provides larger output drive current than the conventional one at a limited area, is implemented. The overall simulation result is better than the conventional double-tail dynamic latched comparator at approximately the same area and power consumption [8].

Wazir Singh et. al., presented CMOS comparators using preamplifier, suitable for high-speed analog-to-digital converters with High-Speed and Low Offset. The designs are mainly optimized for the low propagation time, minimal input resolution and minimal circuit area. Two comparator topologies, namely, double-clock preamplifier based comparator and single-clock preamplifier based comparator have been analyzed and designed. The topologies using preamplifier completely removes the offset that is present in the input of the latched comparator. Nearly 18 mV offset voltage achieved with the structures making them suitable for flash-type and pipeline data conversion applications [9].

Heungjun Jeon et.al., presented a paper, A novel dynamic latched comparator with offset voltage compensation is discussed. The proposed comparator requires one phase clock signal for its operation and can drive a larger capacitive load with a complementary version of the output-latch stage of the conventional comparator design. It provides a larger voltage gain to the regenerative latch, the input referred latch offset voltage is reduced and Metastability characteristic is improved. In addition, with a digitally controlled capacitive offset calibration technique, the offset voltage of the proposed comparator is further reduced to 1.10 mV [10].

Raja Mohd. Noor Hafizi Raja Daud, Mamun Bin Ibne Reaz, and Labonnah Farzana Rahman Soheil Ziabakhsh et. al, presented a novel design of CMOS dynamic latch comparator with dual input single output with the differential amplifier stage using charge sharing topology to achieve low power and high-speed operation. The designed dynamic latch comparator is required for high-speed analog-to-digital converters to get faster signal conversion and to reduce the power dissipation, which are immune to noise. The main challenge lies on the constant speed, which makes more critical; this faster speed has been gained by this proposed designed novel dynamic latch comparator with the combination of resistive dividing comparator and differential current sensing comparator. The topology of the proposed design is able to minimize the propagation delay and power consumption with the improved performances. Even, the different capacitor value and the transistor lengths produced the faster output, which is suitable for the successful operation of the ADC [12].

III. BASIC SUCCESSIVE APPROXIMATION ADC

Successive approximation ADCs is proper choice for low power applications. The successive approximation ADC has been the mainstay of data acquisition for many years. Recent design improvements have extended the sampling frequency of these ADCs into the megahertz region. The architecture of a general SA-ADC usually consists of a rail-to-rail analog comparator, a digital-to-analog converter (DAC) and a successive approximation register (SAR), as shown in Fig.1. In general, the SAR is designed into the digital circuitry. The DAC required in the ADC is designed based on an R-2R ladder. Thus, both of them are suitable for the standard CMOS technology VLSI implementation. However, realizing a high-speed, high-accuracy and rail-to-rail MOS comparator concurrently remains a problem because of MOS device Mismatches and threshold voltage limitations. The input signal of this comparator is expressed by $V_{in} \approx V_{fb}$.

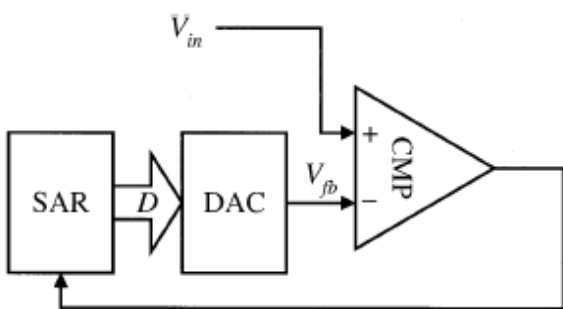
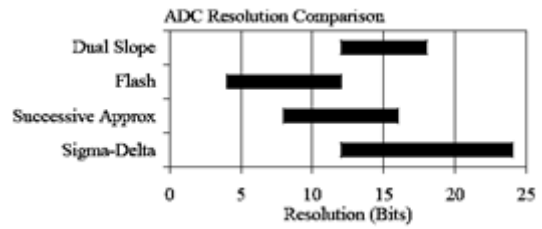


Fig.1: Circuit diagram of a general SA-ADC V_{in} and V_{fb} are the comparator inputs and this symbol \approx denotes the comparator operation. This high-speed, offset compensated and rail-to-rail comparator plays one of the key components for SA-ADC design [4]. Advantages of SA-ADC are power and area-efficient architecture fits well to modern digital CMOS technologies and DAC network is usually capacitive so no static power and its limitation is limited sampling rates.



Type	Speed (relative)	Cost (relative)
Dual Slope	Slow	Med
Flash	Very Fast	High
Successive Appox	Medium – Fast	Low
Sigma-Delta	Slow	Low

Fig.2:ADC types comparison

Figure 2. shows the SA-ADC is capable of high speed, high resolution and reliable, low power and capable of outputting the binary number (one bit at a time) in serial format with that of good trade-off between speed and cost.

IV. COMPARATOR ARCHITECTURES

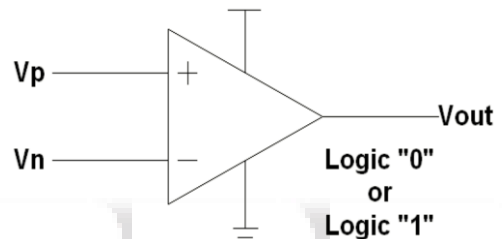


Fig. 3: Comparator Operation

The electrical function of comparator is to generate an output voltage value high and low depending on whether the sign of input voltage is positive or negative.

If $V_P < V_N$ then $V_O = V_{SS} = \text{logic } 0$ and otherwise $V_O = V_{DD} = \text{logic } 1$ as shown in Figure3.

Depending on the nature, functionality and inputs, comparators are classified into different types such as voltage and current comparators, continuous and discrete time comparators and so on. By another classification there are two different kinds of comparators open loop comparator and regenerative comparator.

A. Open Loop Comparator

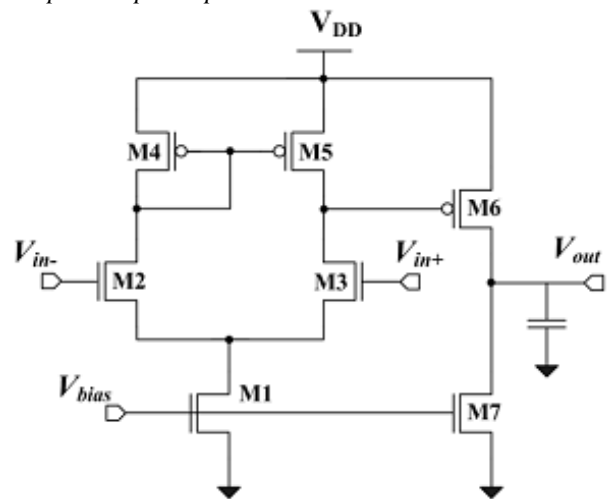


Fig. 4: Open Loop Comparator

Open-loop, continuous time comparators, shown in Figure 4 are an operational amplifier without frequency

compensation to obtain the largest possible bandwidth, hence improving its time response. However, due to its limited gain-bandwidth product, open-loop comparators are too slow for many applications. On the other hand, a cascade of open-loop amplifiers usually has a significantly larger gain-bandwidth product than a single-stage amplifier with the same gain. However, since it costs more area and power consumption, cascading does not give practical advantages for many applications.

B. Regenerative Comparator:

Regenerative comparators use positive feedback to accomplish the comparison of two signals. This comparator is also known as latch with two cross-coupled MOSFETs as shown in Figure 5(NMOS latch) and Figure 6(PMOS latch). Two phase clock is used to determine its modes of operation. Latches have a faster switching speed and the propagation delay of the regenerative comparator is slow at the beginning and speeds up rapidly as time increases.

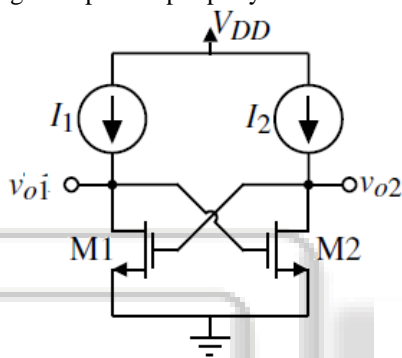


Fig. 5: NMOS latch

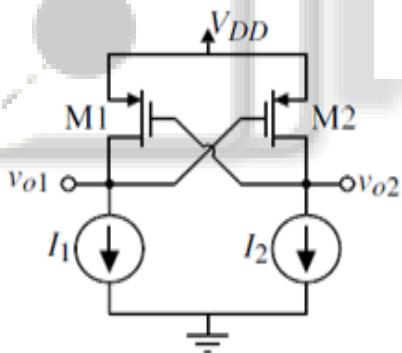


Fig. 6: PMOS latch

C. High Speed Comparators:

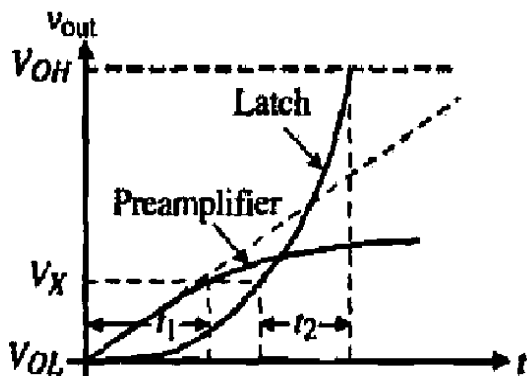


Fig. 7: Preamplifier and latch step response

High speed comparator consists of open loop and

regenerative comparator. It mainly consists of three blocks, Input stage, a flip flop and S R latch. This architecture combines the best aspects with a negative exponential rise due to preamplifier stage and positive exponential rise due to latch stage as shown in Figure 7. The basic principle behind this high speed comparator is to get minimum propagation delay, fast speed and low input referred voltage which can be achieved by using a pre amplifier by building up the input change to a sufficiently large value and then apply it to the latch for quick transition to the full binary output.

D. Dynamic Latch Comparator:

A dynamic latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. A simple dynamic latch is shown in Fig 8. The circuit is driven by a clock. During one phase of the clock (clk =1) when the transmission gate is closed, the latch acts transparent, and the inverter is directly connected to the input. In the other phase of the clock (clk = 0), the transmission gate opens and the inverter's output is determined by the node. Setup and hold times determined by the transmission gate must be taken in consideration in order to ensure proper operation of the latch i.e. adequate level of voltage is stored on the gate capacitance of the latch.

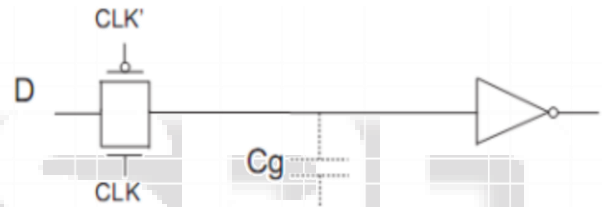


Fig. 8: Dynamic latch

1) Pre-Amplifier Latch based Comparators:

Pre-amplifier based comparator i.e. a comparator having a preamplifier followed by a regenerative latch stage which is again followed by an output buffer as shown in Figure 9 shows block diagram of pre-amplifier latch comparator.

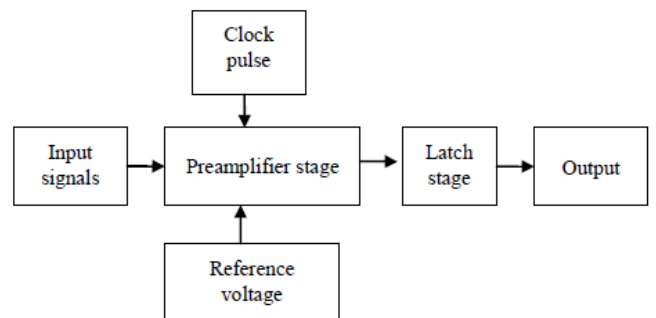


Fig. 9: Pre-amplifier latch comparator

More practically, the input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output-latch stage as shown in Figure 10 and figure 11 (two type of pre-amplifier based latch comparator). Preamplifier based latched comparator is a combination of a pre-amplifier and a latch. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage. In addition, by using pre-amplification stage it reduces the kickback noise as well as solves the meta-stability problem.

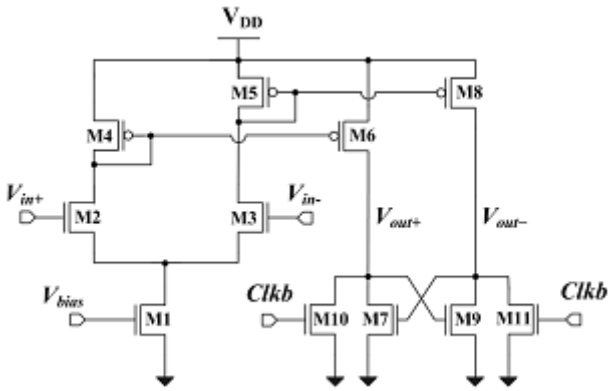


Fig. 10: A static Latched Comparator

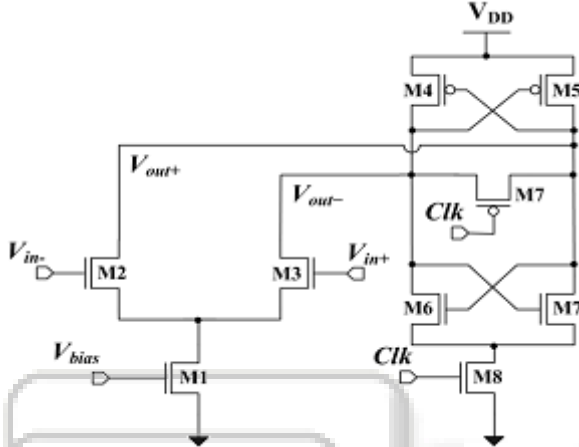


Fig. 11: A Class AB Latched Comparator

Pre-amplifier latch based comparators suffers not only from large static power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain-to-source resistance due to the continuous technology scaling. Therefore, for the high-speed low power CMOS applications, a dynamic comparator without pre-amplifier is highly desirable. This can be realized in terms of a dynamic comparator with digital offset calibration techniques.

2) Resistor Divider Comparator (Lewis Gray Comparator):

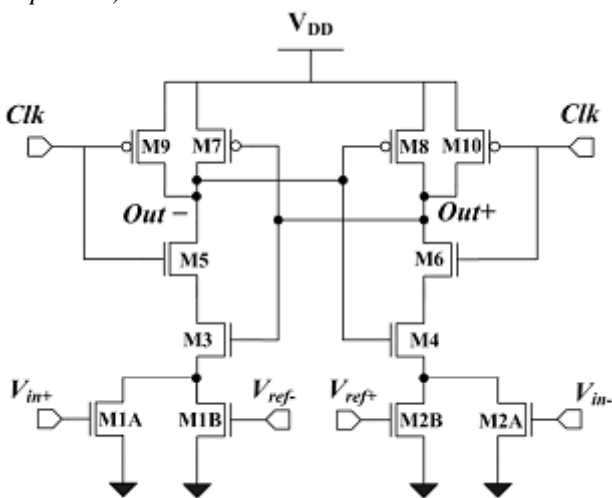


Fig. 12: Resistor Divider Comparator

Figure 12 shows Lewis-Gray comparator. Since the input transistor M1A/B and M2A/B operate in the triode region and act like voltage controlled resistors, this comparator is called "Resistive Divider Comparator." The advantage of

this comparator is its low power consumption (No DC power consumption) and adjustable threshold voltage (decision level) since Lewis-Gray comparator shows a high offset voltage and its high offset voltage dependency on a different common mode voltage V_{com} , it is only suitable for low resolution comparison.

3) Differential Pair/Latch-Type SA Comparator:

Figure 13 shows differential pair comparator.

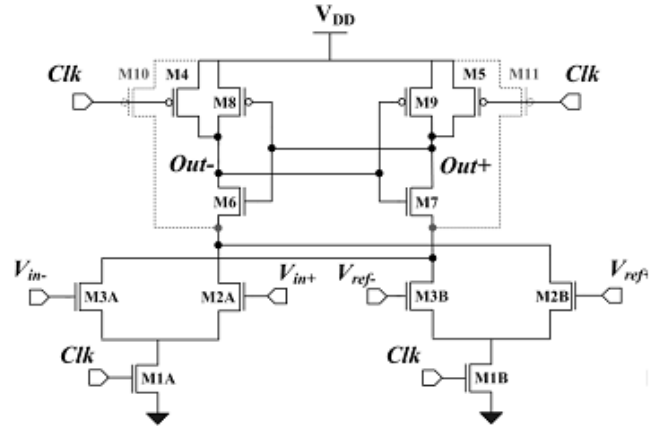


Fig. 13: Differential Pair Comparator

Similar to resistor divider comparator this comparator has an adjustable threshold voltage. This comparator shows faster operation and less overall offset voltage comparing to Lewis Gray comparator. For the analysis we consider its simplified form as shown in Figure 14 latch type SA comparator.

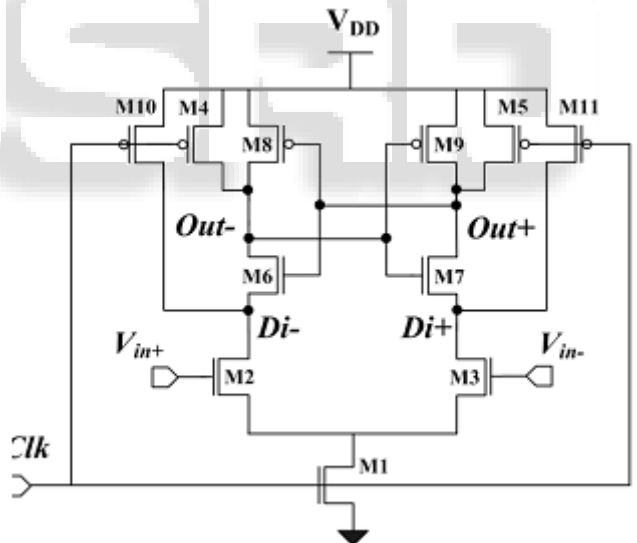


Fig. 14: Latch-type Voltage SA (sense amplifier) Comparator

Latch type sense amplifiers are used to read the contents of the different kinds of memory, A/D converters, data receivers and on-chip transistors since they yield fast decision due to positive feedback. These are very effective comparators. The circuit diagram of the latch type voltage sense amplifier that uses back to back latch stage to generate positive feedback. Since its structure which consists of a stack of 4 transistors requires large voltage headroom and also speed and offset of this SA is very much dependent on the common mode voltage of the input, it is problematic in low-voltage deep-submicron CMOS technologies.

V. DESIGN PARAMETER OF LATCH COMPARATOR

- Accuracy (offset, noise, resolution)
- Settling time (tracking BW, regeneration speed)
- Sensitivity (gain)
- Metastability (any decision is better than no decision!)
- CMRR
- Power consumption

A. Performance Characteristics:

- *Voltage gain (A_v)* - Differential DC gain of a comparator.
- *Input offset (V_{os})* - Voltage that must be applied to the input to obtain a transition between the low and the high state.
- *Response time (t_r)* - Time interval between the instant when a step input is applied and the instant when the output reaches the corresponding logic level (depends on the input step amplitude).
- *Comparison rate*- Comparison rate is the highest frequency in which a comparator results in a correct value and is defined by the overdrive recovery test. Comparison rate depends on the speed.

B. Comparator Gain and Response Time

Basic Considerations

- A comparator is basically an open loop gain stage
- Any gain stage can be used as comparator, from a simple inverter to a complex operational amplifier.
- If required a latch can be connected at the output of the gain.

Key issues in comparator design

- Gain obtained by using a single complex stage or by using a cascade of simple stages.
- Offset cancellation.
- Power supply rejection.
- Overdrive Recovery
- Power Consumption

C. Offset Voltages Cancellation Technique in Dynamic Comparator:

Dynamic comparators are widely used in the high speed ADCs due to its low power consumption and fast speed. However, there is a lack of thorough traditional comparator is built by an operational amplifier the calculation of offset voltage is straightforward since the operation regions of all transistors are well defined. To overcome this difficulties the operation regions and bias conditions of transistors in a dynamic comparator when the mismatch exists, a balanced method is used that is to calculate the input offset voltage. The input-referred offset voltage, defined as input level that forces output voltage to go to zero.

Effect of offset on Comparator: minimum amount of gain preceding comparator. Use of preamp before latch advantage of reducing the input offset voltage of latch by the gain of pre-amplifier. Of the various offset cancellation methods, two of the most common approaches, based on offset cancellation techniques are used based on input offset storage (IOS) and output offset storage (OOS).

These two approaches, applied to a fully differential comparator. Each of these topologies comprises a pre amplifier, offset storage capacitors and a latch. In this

method, a voltage equal to the input offset voltage is virtually applied to one of the inputs of the comparator to cancel the mismatch effects and make. Circuit techniques to reduce offset different circumstances require different approaches. Fall into 3 categories:

- 1) Cancellation
- 2) Sampling
- 3) Modulation

Comparator offset cancellation

- Cancellation in preamplifier
- Cancellation in Latch

D. Challenges in Low Power Design:

- Power Dissipation
- Low Power Design Space
- Low Voltage Supply
- Switching Activity
- Physical Capacitances

There are many no. of approaches that can be used to reduced power consumption remaining with in dimensions of designing complex circuitry for low power; for that design has to be optimized by three parameter those are Power, Performance and Area.

By following these various points we can achieve low power design.

- A low supply voltage and circuit design technique, targeting the supply voltages are taken around 1 Volt or lower than 1V and operating with reduced thresholds voltage.
- Low power interconnect, using reduced activity or advanced technology, reduced swing approaches.
- Dynamic power management techniques are varying with the supply voltage and the execution of design speed according to activity measurements. This can be achieved by the whole design should be divided into sub-circuits whose energy levels also can be independently controlled and by powering down sub-circuits which are not in used.

VI. APPLICATIONS

- 1) N. Naga Sudha designed a High Speed and Low Power Dynamic Latch Comparator for PTL Circuit Applications this design of high-speed and low power dissipating clocked comparator for stack circuit applications. The comparator is attractive for the applications where both speed and power consumption are of the highest priority [1].
- 2) S. Yewale and R. Gamad presented an improved method for design of CMOS comparator based on a preamplifier-latch circuit driven by a clock. This design is implemented in Sigma-delta Analog-to-Digital Converter (ADC). Thus, by considering factors of speed and resolution, preamplifier latch comparator are the choice for a high speed analog to digital converter. This type of latched comparator was also used for high speed and reduced power dissipation comparator performance [3].
- 3) S. Rahil Hussain, et.al, presented a High Speed and Low Power Dynamic Latched Comparator for Aircraft Application. These types of comparators are used in aircraft applications. The simulation results of three comparators show that the dynamic latched comparator will occupy less active area and also having higher speed

of operation and consumes less power. So by using the dynamic latched comparator in the application of aircraft is more efficient when compared to other comparator designs [6].

VII. SUMMERY

In this paper offset cancellation techniques, key issues in comparator design, performance characteristics and challenges that are faced in designing low power comparators are discussed as the comparator action depends upon various factors like power supply, technology, area etc. However of various things our aim is to achieve a low power design with high speed so compromise with other factors is to be made. A low-power and low-offset dynamic comparator using the offset cancellation technique auto zeroing and hysteresis is proposed. Response of the comparator can be improved by adding hysteresis equal to or greater than the amount of the largest expected noise amplitude. Reducing propagation delay speed can be increased. Low power, low offset voltage, minimum propagation delay and high speed are the essential factors for high performance ADCs.

REFERENCES

- [1] N. Naga Sudha et. al, "High Speed and Low Power Dynamic Latched Comparator for PTL Circuit Applications"/International Journal of Computer Science and Information Technologies, (IJCSIT) Vol. 3 (1), pp-2982 – 2991, 2012.
- [2] Mehdi Banihashemi, K. Hadidi, And A. Khoei, "A Low Power, High Resolution, 6 MHz Comparator," ECCTD 01, August 28-31, 2001, Espo, Finland.
- [3] S. Yewale and R. Gamad, "Design of Low Power and High Speed CMOS Comparator for A/D Converter Application", *Wireless Engineering and Technology*, Vol.3, pp. 90-95, 2012.
- [4] Chi-Sheng Lin and Bin-Da LIU , Senior Member, "A New Successive Approximation Architecture for Low Power Low Cost CMOS A/D Converter" IEEE Journal of solid-state circuits, Vol.38, NO.1, pp.54-62, January 2003
- [5] B. Razavi, and B. A. Wooly, "Design techniques for high-speed, high-resolution comparators," *IEEE J. Solid -State Circuits*, vol. 27, pp. 1916-1926, Dec. 1992.
- [6] S. Rahil Hussain, N. Naga Sudha, V. Narasimha Nayak, Dr. Fazal Noor Basha, "High Speed and Low Power Dynamic Latched Comparator for Aircraft Application" / International Journal of Engineering Research and Applications (IJERA) Vol. 2, Issue 3, , pp.1301-1312, May-Jun 2012
- [7] Yavuz Değerli, Nicolas Fourches, Michel Rouger, and Pierre Lutz. "Low-Power Auto zeroed High- Speed Comparator" IEEE Transaction on Nuclear Science vol. 50 no.-5 oct.2003.
- [8] Heung Jun Jeon, "Low-power high-speed low-offset fully dynamic CMOS latched comparator", Northeastern University, Department of and Computer Engineering, January 2010.
- [9] Wazir Singh, "Study and Design of Comparator High Speed ADCs", Thapar University, Patiala, Department of Electronics and Communication Engineering, July-2011.
- [10] Heungjun Jeon and Yong-Bin Kim, "A Novel Low-Power, Low-Offset and High-Speed CMOS Dynamic Latched Comparator", IEEE press, 2010.
- [11] B. Goll and H. Zimmermann, "A Comparator with Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65V," *IEEE Transactions on Circuits and System II: Express Brief*, vol. 56, no. 11, pp. 810-814, Nov 2009.
- [12] Raja Mohd . Noor Hafizi Raja Daud, Mamun Bin Ibne Reaz, and Labonnah Farzana Rahman, " Design and Analysis of Low Power and High Speed Dynamic Latch Comparator in 0.18 μ m CMOS Process", *IJIEE Vol. 2, No. 6, pp. 944-947, November 2012.*