The Impact of Short Channel Effects MOSFET’s Characteristics Due to variation in Threshold Voltage

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Abstract—to get the higher speed, low power dissipation and higher packing density MOS integrated circuits, the dimensions of MOSFETs have continued to shrink, which is done by scaling. With the scaling of MOSFETs into deep-sub micrometer regime, non-ideal effect is becoming a resurgent hot topic in the reliability community. One of the non-ideal effects is the expected increase in threshold voltage variation due to worsening short channel effect. In this paper we analyzed the role of substrate (the body effect) on the threshold voltage. The variation in MOSFET threshold voltage will affect the dynamic, static characteristics and or the short-channel effect (SCE). The most important parameters of a MOSFET are its channel length, the distance between the source and drain. It has been recognized that short-channel MOSFETs offer both speed and density advantages over their long-channel counterparts. In a given generation of technology, however, there is a minimum channel length below which the gate starts to lose control of the MOSFET current. The short channel prevention circuit uses physically meaningful parameters provides an easy way for technology benchmarking and performance projection.

I. INTRODUCTION

To get the higher speed, low power dissipation and higher packing density MOS integrated circuits, the dimensions of MOSFETs have continued to shrink, which is done by scaling. By the technology scaling the MOSFET’s channel length is reduced. As the channel length approaches the source-body and drain-body depletion widths, the charge in the channel due to these parasitic diodes become comparable to the depletion charge due to the MOSFET gate-body voltage, rendering the gate and body terminals to be less effective. With the scaling of MOSFETs into deep-sub micrometer regime, non-ideal effects are becoming a resurgent hot topic in the reliability community. When the channel length reduces to dimension below which the gate starts to lose control of the MOSFET current due to the increased charge sharing from source/drain. SCE leads to several reliability issues including the dependence of device characteristics, such as threshold voltage, upon channel length. The threshold voltage VT for a MOS transistor can be defined as the voltage between the gate and the source terminals below which the drain to source current effectively drops to zero. This leads to the scatter of device characteristics because of the scatter of gate length produced during the fabrication process.

II. SUBSTRATE BIAS (BODY) EFFECTS

Due to the reverse biased channel to substrate p-n junction the channel width becomes reduces by increase in threshold voltage is called as Substrate Bias Effect in Body-Tied MOSFET’s. It shows that the threshold voltage of the characteristics does not change very much as the body is reverse-biased, while it becomes lower as the body is forward-biased. The threshold voltage VT is not a constant with respect to the voltage difference between the substrate and the source of the MOS transistor. This effect is called the body effect or substrate bias effect. The threshold voltage becomes higher as the body is reverse-biased and stops rising when the body bias exceeds a certain value, while the threshold voltage becomes lower as the body is forward-biased. It also shows the dependence on the channel impurity concentration, drain voltage, and gate length. It is clear that a higher impurity concentration requires a higher body-bias to reach a constant threshold voltage. The higher drain bias and a shorter gate length decrease the body bias for the threshold voltage saturation. We think that this is because it is easy for the body region near the drain edge to become fully depleted by the drain bias and this affects all the characteristics of the short-channel device. In addition, when the threshold voltage becomes constant with a reverse body-bias, the - factor simultaneously becomes small and constant.

III. THE IMPACT OF VARIATION IN THRESHOLD VOLTAGE

Supply voltage (Vdd) and threshold voltage (Vt) scaling is the most effective approach to keep active power dissipation under control while maintaining performance improvement. One of the limits to Vdd scaling is the expected increase in Vt variation. In this work a CMOS layout model will be developed for existing circuit technique that adaptively biases the body terminal of MOSFET devices to control this threshold voltage variation. It will show that as MOSFET technology is scaled, the body bias required for compensating die-to-die Vt variation increases, which in turn further increases SCE, and, because of this increase in SCE, within-die Vt variation becomes worse. It will also be shown that the die that requires larger body bias to match its mean Vt to the target Vt will end up with a higher within-die Vt variation. The resulting increase in within-die Vt variation due to adaptive body bias can impact clock skew, worst-case gate delay, worst-case device leakage current, total chip leakage power, and analog circuit performance.

The threshold voltage Vth does vary with the voltage difference Vd between the source and the body (substrate). Thus including this difference, the generalized expression for the threshold voltage is reiterated as

$$Vt = V_{t0} + (2\varepsilon_s q N_A)\frac{1}{2}Cox \left[ \frac{(2\Omega_F + V_{sb})^{1/2} - (2\Omega_F)^{1/2}}{2} \right]$$

in which the parameter Y, known as the substrate-bias (or body-effect) coefficient is given by
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\[ Y = \sqrt{\frac{2qN_a \varepsilon_s}{C_{ox}}} \]

\[ = \frac{(2*1.6*10^{-9} * 11.7*80854*10^{-14} * 10^{14})^{1/2}}{1.7265*10^{-7}} \]

\[ = 0.03334 \]

Where,

\[ N_a = 3*10^{16} \]

\[ T_{ox} = 200*10^{-8} \]

\[ \varepsilon_{ox} = 11.7*8.854*10^{-14} \]

\[ C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \]

\[ = 3.9*80854*10^{-14} / 200*10^{-8} \]

\[ Y = \frac{(2*1.6*10^{-9} * 11.7*80854*10^{-14} * 3*10^{16})^{1/2}}{C_{ox}} \]

\[ = 0.57 \]

\[ \Omega F = \frac{K T}{q \ln (N A/n I)} \]

\[ = 1.38*10^{-23} * 300/1.6*10^{-19} \ln (10^{14} / 1.5*10^{10}) \]

\[ = 0.228 \text{ V} \]

\[ V_t = V_t^0 \]

Then, at \( V_{sb} = 2.5 \text{ volts} \)

\[ V_{T1.5} = V_{T0} + 0.57 \left( \sqrt{0.75 + 2.5} - \sqrt{0.75} \right) = V_{T0} + 0.57 \]

As is clear, the threshold voltage increases by almost half a volt for the above process parameters when the source is higher than the substrate by 2.5 volts.

A MOSFET transistor is defined as a short-channel device if its channel length is on the same order of magnitude as the depletion regions thicknesses of source and drain junction. Otherwise MOSFET can be defined as a short-channel device if effective channel length \( L_{eff} \) is approximately equal to the S and D junction depth \( x_j \). When NMOS is defined as a short-channel device the length of channel will have impact on the threshold voltage.

A short-channel will reduce the threshold voltage of \( \Delta V_t \) compare with long-channel device.

\[ V_t^0 \text{ (short-channel)} = V_{t0} - \Delta V_t^0 \]

A MOSFET transistor is defined as a narrow-channel device if its channel width is on the same order of magnitude as the maximum depletion regions thickness into the substrate \( (x_{dm}) \). This effect will have influence in the threshold voltage and results in higher value for \( O \text{Vt}^0 \) if compared with long-channel device.

\[ V_t^0 \text{ (narrow-channel)} = V_{t0} + \Delta t_0 \]
IV. CONCLUSION

In this paper, we show that the non-idealities on the MOSFET characteristics strongly depend on the transistor aspect ratio and in particular on the transistor channel width, so that even digital applications may be strongly disturbed by these effects. Due to the reverse biased channel to substrate p-n junction the channel width becomes reduces by increase in threshold voltage is called as Substrate Bias Effect in Body-Tied MOSFET’s. The drain to source current varies from 2.518mA to 2.071mA due to variation in body bias potential for short channel and drain to source current varies from 1.718mA to 0.1mA due to variation in body bias potential for long channel. The power dissipation of 15µW and maximum drain to source current through circuit is 0.212mA.

REFERENCES


