Multiple Channel Serial I/O Interfacing using FPGA Kit

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Abstract—The Digital input and output interface (DIO) could be an important part for a machine needed to be interacted with its setting. Even though a main processing unit (MPU) utilized within the machine has its own DIO channel, for some cases, the machine should use plenty of DIO channel than those the MPU can offer. To avoid this downside, a DIO board interfaced on to the MPU via serial communication is intended. If the MPU connect with multiple DIO boards directly, it's going to waste sometime to process of communication data. The inessential measure of the MPU and likelihood to have many DIO boards connected, a serial interface unit supported FPGA is developed to help the MPU to talk with DIO boards. The FPGA unit automatically browses serial signals from each DIO boards and save understood data to share registers for MPU to scan. The FPGA unit put together impromptu reads registers written by MPU and send registers values to DIO boards automatically.

Keywords: DIO, MPU, Interface, FPGA

I. INTRODUCTION

In general, a machine has a minimum of one digital input or output unit to move with alternative machines or its atmosphere. Most the time, MPU features a limit range of input and output channel, that is often but the machine wants. A method to avoid this downside is to possess a DIO board connecting to the MPU via serial communication. Rather than victimization thirty two pins for thirty two input channels, solely four pins for a serial communication for required for MPU to interface with DIO board

A communication exploitation serial protocol is time overwhelming. The communication between MPU and DIO boards in signal hand checking before receiving or transmitting information generally consumes plenty of our time from the MPU. To avoid these issues, a middleware unit has been enforced on FPGA to handle communication tasks between the MPU and DIO boards. Whereas the FPGA unit communicates with DIO boards via serial interfaces, share registers area unit want to link between the FPGA unit and MPU.

FPGA is wide used to implement a middleware unit. It's enforced to be a SPI master for a microcontroller unit (MCU) to speak with SPI Slave. By exploitation SPI protocol, it links between DSP and wireless radio. It's want to browse four channels ADC using four completely different protocols that are parallel, SPI, and one-wire protocol, and communicates with computer by USB controller. Flexray controller on FPGA for intra-vehicular communication is enforced.

In this paper, I introduce a development of FPGA unit that automatically write and browse information from multiple DIO boards via serial communications and also the MPU via share registers. Having the FPGA unit, it helps to cut back the burden of a serial communications between the MPU and DIO boards and additionally increase variety of DIO boards that the MPU will connect with. I selected to implement the FPGA unit and program it by VHDL language.

In this article, I will explain protocol to communicate with DIO board and will introduce implementation of automatic multi-channel serial I/O interface on FPGA.

II. INTERFACING

The interfacing requirements for a serial I/O peripheral are the same as for a parallel I/O device. The microprocessor identifies the peripheral through a port address and enables it using the read or write control signals. The primary difference between parallel I/O and serial I/O is in the number of lines used for data transfer- The parallel I/O uses the entire data bus and the serial I/O uses one data line. Fig. 1 shows a typical configuration of serial I/O transmission. The MPU chooses the peripheral through chip select and uses the management signals scan to receive information and write to transmit information. The address secret writing is either peripheral I/O or memory mapped I/O. Similarly, a serial peripheral can be interfaced under either program control or interrupt control. Serial communication uses Synchronous Data Transmission as well as asynchronous Data Transmission. In Synchronous Data Transmission, the transmitter and receiver are synchronized whereas asynchronous Data Transmission occurs at any time.

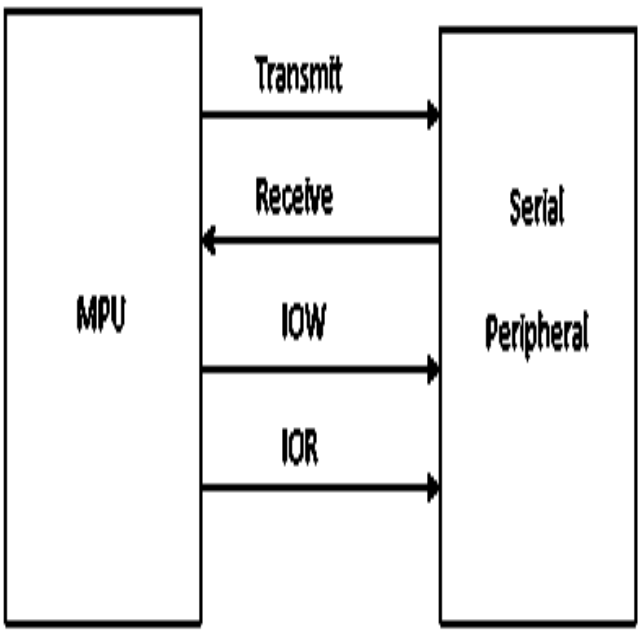

Fig. 1: Block diagram of Serial Input Output Interfacing

III. ERROR CHECKING

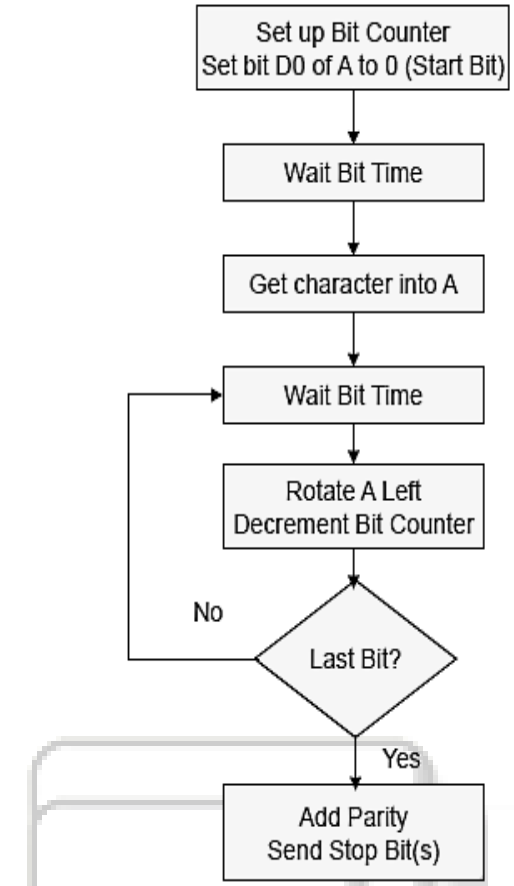

Fig. 2: Flowchart for serial Transmission

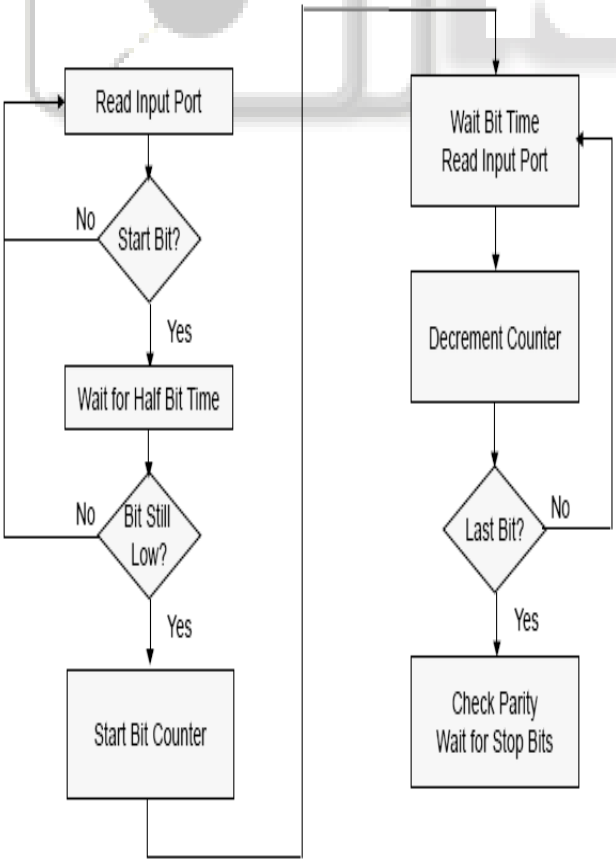

Fig. 3: Flowchart for serial Reception

Various types of errors may occur during transmission. To allow checking for these errors, extra data is transmitted with the info. Error checking techniques are parity checking and verification. But in this article checksum (CS) method is used when larger blocks of data are being transmitted combined flowchart for error checking and in transmission and Reception of serial data is shown in figure 2 and 3.

IV. INCREASING INPUT-OUTPUT CHANNEL BY USING SERIAL INTERFACE

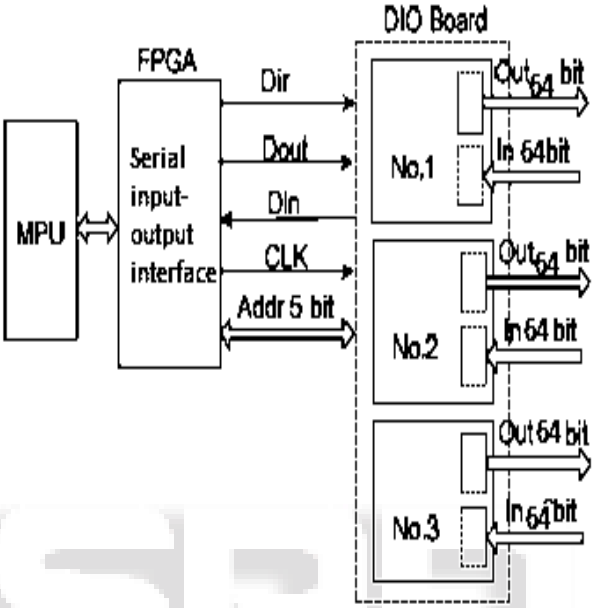

Fig. 4: Serial interfacing between FPGA kit and digital input-output board

In industrial machine, most of MPU pins are used to communicate with several peripheral elements. Therefore, there's not abundant MPU pin left for different use. To manage machine with several input-output (I/O) channels, the quantity of I/O to regulate I/O device is required to be sufficiently enhanced. Rather than directly connecting between MPU pins and I/O pins, DIO boards can communicate with MPU via FPGA by using serial protocol as showed in Fig. 4.

In Fig. 4 the Dir-signal defines a direction of a communication signal. Dir is 1 as FPGA send data to DIO board. Dir is 0 as FPGA receive data from DIO board. CLK-signal defines a synchronize of communication and works at rising edge. Whilst Dout-signal is used to send data from FPGA to DIO boards, Din-signal is used to receive data from DIO boards to FPGA. Addr-signals represent an address of DIO board that the FPGA unit wants to communicate with.

Input and signaling diagrams are shown in Fig 5. To send out information (Data Out), a most significant bit (MSB) is first sent. 0-bit to 63-bit are sent from the FPGA unit to DIO board whereas 64-bit to 67-bit area unit checking bits (Check Sum-CS) for data correction. To get information (Data In), MSB is received before a low significant bit (LSB). 0-bit to 7-bit are Check sum, whereas 8-bit to 71-bit are information sent from DIO board to the FPGA unit. Addr-signals shows sequence of communication in different DIO boards.

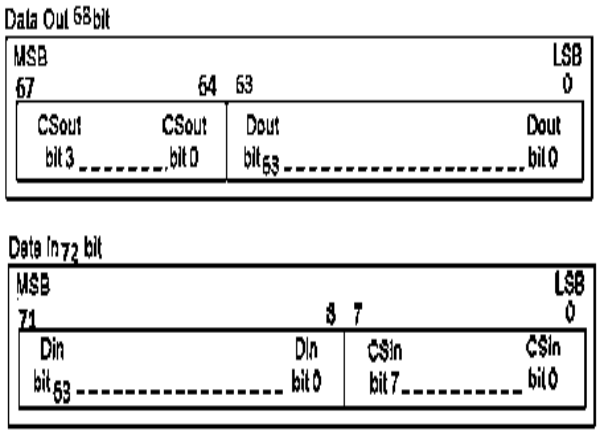

Fig. 5: I/O signal Diagram

V. COUNTER USED IN SERIAL I/O INTERFACE ON FPGA

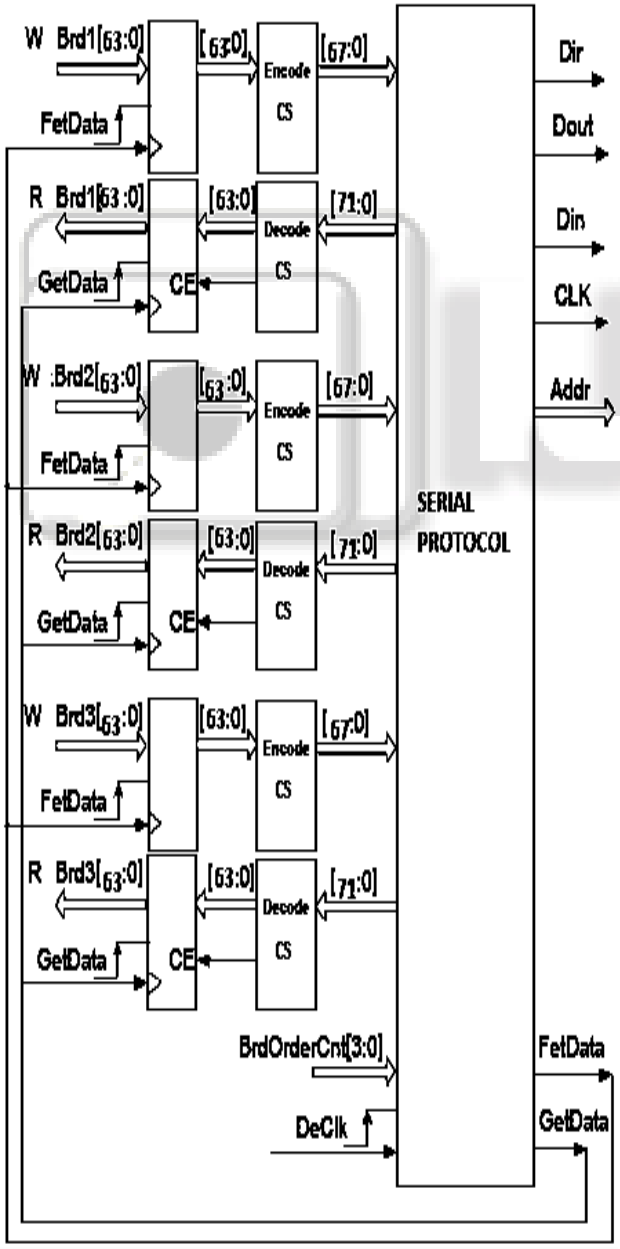

Fig. 6: Multiple channel serial input output interfacing with Digital input-output boards on FPGA

VI. CONCLUSION

In implementation of automatic multi-channel serial I/O interface on FPGA, first we generate sequential counter which are "BrdOrderCounter" and "BrdCounter". The "BrdOrderCounter" is sequential counter of DIO boards, which mean "BrdOrderCounter" counts 0 to 5. The "BrdCounter" is sequential counter of serial state machine, in this propose state of serial in each board have one hundred and twenty four states.

In Fig. 6 shows structure of Automatic multi-channel serial I/O interface with DIO boards on FPGA. The "W Brd" is 64-bit register of output data on board1. We latch "W Brd" register by rising edge of "FetData" signal from "Serial Manager" and then send to "Encode CS" for adding check sum to output data so that it becomes 68 bits. The "R Brd1" is 64-bit register of input data on board1. The "R Brd1" is 64-bit register coming from "Decode CS", which is for check sum decoding of 72-bit input data and input data correction. We latch "R Brd1" register by using two signals. The two signals are rising edge of "GetData" signal from "Serial manager" and check sum correction signal. The check sum correction signal enables the latch.

We have developed the FPGA unit for linking between the MPU and DIO boards. It communicates with DIO boards via the serial protocol. Whereas share registers is employed to speak with the MPU the FPGA unit mechanically scans serial signals from every DIO boards and save taken information to share registers for MPU to read. The FPGA unit additionally spontaneously reads registers written by MPU and send registers values to DIO board mechanically. Time interval for handling the serial protocol within the MPU is reduced and additionally the MPU will hook up with multiple DIO boards at a similar time

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