

A Single-Phase Clock Multiband Low-Power Flexible Divider

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Abstract—In this paper, a low-power single-phase clock multiband flexible divider for Bluetooth, Zigbee, and IEEE 802.15.4 and 802.11 a/b/g WLAN frequency synthesizers. The frequency synthesizer was implemented using a charge-pump based phase-locked loop with a tri-state phase/frequency detector and a programmable pulse-swallow frequency divider. Since the required frequency of operation can be as high as 1.4GHz, the speed of the digital logic used in the frequency divider is a critical design factor. A custom library of digital logic gates was designed using MOS current-mode logic (MCML). These gates were designed to operate at frequencies up to 1.4GHz. This report outlines the design of the phase/frequency detector and the programmable pulse-swallow frequency divider. The design, layout, and simulation of the MCML logic family are also presented.

Key Words: DFF, dual modulus prescaler, dynamic logic, E-TSPC, frequency synthesizer, high-speed digital circuits, true single-phase clock (TSPC), wireless LAN (WLAN).

I. INTRODUCTION

Wireless LAN (WLAN) in the multi gigahertz bands, such as HiperLAN II and IEEE 802.11a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like IEEE 802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer. The integrated synthesizers for WLAN applications at 5 GHz reported in [1] and [2] consume up to 25mW in CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range. The best published frequency synthesizer at 5 GHz consumes 9.7mW at 1-V supply, where its complete divider consumes power around 6mW [3], where the first-stage divider is implemented using the source-coupled logic (SCL) circuit [4], which allows higher operating frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers. The TSPC [5] and E-TSPC [6] designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem [5]. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5 GHz [7], [8]. The frequency synthesizer reported in [6] uses an E-TSPC prescaler as the first-stage divider, but the divider consumes around 6.25mW. Most IEEE 802.11a/b/g frequency synthesizers

employ SCL dividers as their first stage [3], [9], while dynamic latches are not yet adopted for multiband synthesizers. In this paper, a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler [10] and a wideband multi-modulus 32/33/47/48 prescaler as shown in Fig. 1. The divider also uses an improved low-power loadable bit-cell for the Swallow S-counter.

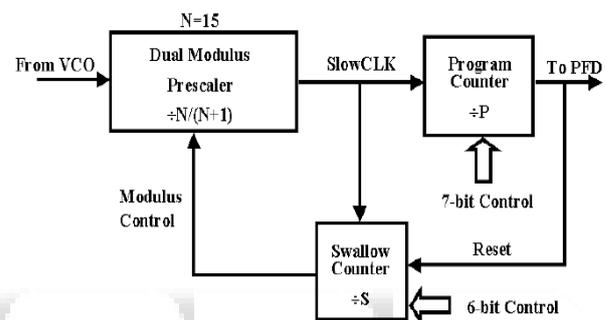


Fig. 1: Proposed dynamic logic multiband flexible divider.

II. DESIGN CONSIDERATIONS

The key parameters of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated by the method described in [11] and is given by

$$f_{\max} = \frac{1}{t_{pLH} + t_{pHL}} \quad (2.1)$$

Where t_{pLH} and t_{pHL} are the propagation delays of the low-to-high and high-to-low transitions of the gates, respectively. The total power consumption of the CMOS digital circuits is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{\text{switching}} = \sum_{i=1}^n f_{\text{clk}} C_{Li} V_{dd}^2 \quad (2.2)$$

Where n is the number of switching nodes, f_{clk} is the clock frequency, C_{Li} is the load capacitance at the output node of the i th stage, and V_{dd} is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{sc} = I_{sc} * V_{dd} \quad (2.3)$$

Where I_{sc} is the short-circuit current. The analysis in [12] shows that the short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18- μ m CMOS process.

III. WIDEBAND E-TSPC 2/3 PRESCALER

The dual-modulus prescaler (DMP) divides the VCO frequency by either N , or $N+1$, depending on the value of modulus control. In this project, N was chosen to be 15 and the circuit was designed to divide by 16 when modulus control is low and by 15 when modulus control is high. The DMP was designed as a finite state machine with 16 possible states. Four flip-flops were required to generate the 16 states, and next-state generation logic was used to cycle through the states on each cycle of the input signal from the VCO. The implementation of the DMP is provided in fig. 2. When the modulus control signal is low, all 16 states are possible; however, setting modulus control high causes the circuit to skip the zero state. Since only 15 states are used, the DMP divides by 15 when the modulus control signal is high. The use of the differential MCML logic gates is evident.

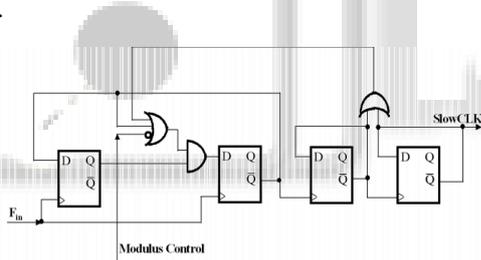


Fig. 2: Implementation of a 15/16 Dual-Modulus Prescaler

In addition, the three-input OR gate indicated in Figure 2 was implemented using 2 two-input OR gates. Figure 3 provides the simulation results for the DMP with modulus control set to logic '0'. As expected, the frequency of Slow CLK is equal to the input frequency divided by 16. These results suggest that the dual-modulus prescaler operates as designed and intended.

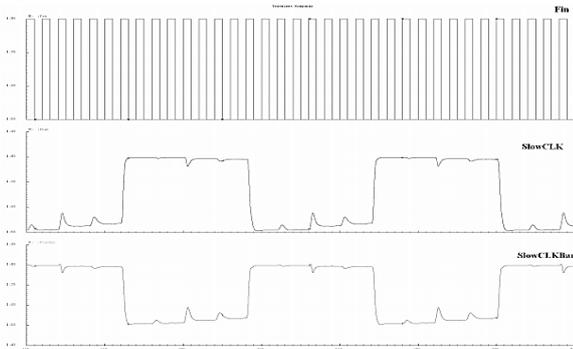


Fig. 3: Simulation Results for the Dual Modulus Prescaler (Modulus Control =0)

IV. MULTIMODULUS 32/33/47/48 PRESCALER

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 4. It is similar to the 32/33 prescaler used in [7], but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (di-vide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider which will be discussed in Section V. The multimodulus prescaler consists of the wideband $2/3(N_1/N_1+1)$ prescaler [10], four asynchronous TSPC divide-by-2 circuits ((AD) =16) and combinational logic circuits to achieve multiple division ratios. Besides the usual Signal for controlling (N_1/N_1+1) divisions, the additional control signal Set is used to switch the prescaler between 32/33 and 47/48 modes.

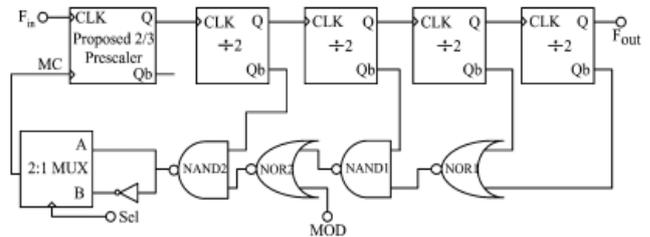


Fig. 4: Proposed multimodulus 32/33/47/48 Prescaler.

A. Case 1: $Set=0$

When $Set=0$, the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal. If $MC=1$, the 2/3 prescaler operates in the divide-by-2 mode and when $MC=0$, the 2/3 prescaler operates in the divide-by-3 mode. If $MOD=1$, the NAND2 gate output switches to logic "1" ($MC=1$) and the wideband prescaler operates in the di-vide-by-2 mode for entire operation. The division ratio N performed by the multimodulus prescaler is

$$N = (AD \times N_1) + (0 \times (N_1 + 1)) = 32 \quad (3.1)$$

Where $N_1=2$ and $AD=16$ is fixed for the entire design. If, for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the divide-by-3 mode. The division ratio $N+1$ performed by the multimodulus prescaler is

$$N + 1 = ((AD - 1) \times N_1) + (1 \times (N_1 + 1)) = 33 \quad (3.2)$$

B. Case 2: $Set=1$

When $Set=1$, the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD . If $MC=1$, the 2/3 prescaler operates in divide-by-3 mode and when $MC=0$, the 2/3 prescaler operates in divide-by-2 mode which is quite opposite to the operation performed when $Set=0$. If $MOD=1$, the division ratio $N+1$ performed by the multimodulus prescaler is same as (4) except that the wideband prescaler operates in the divide-by-3 mode for the entire operation given by

$$N + 1 = ((AD \times (N_1 + 1)) + (0 \times (N_1))) = 48 \quad (3.2)$$

If MOD=1, the division ratio N performed by the multimodulus prescaler is

$$N = ((AD - 1) * (N_1 + 1)) + (1 \times N_1) = 47 \quad (3.3)$$

V. MULTIBANDFLEXIBLEDIVIDER

The single-phase clock multiband flexible divider which is shown in Fig. 1 consists of the multimodulus 32/33/47/48 prescaler, a 7-bit programmable S-counter and a 6-bit swallow P-counter. The multi modulus 32/33/47/48 prescaler is briefly discussed in Section IV. The control signal Sel decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5–5.825 GHz).

A. Program Counter

The program counter is responsible for counting P pulses of Slow CLK before outputting a pulse to the phase/frequency detector and resetting itself and the swallow counter. The implementation used in this project, using a 7-bit ripple counter, a 7-bit comparator, and a zero-detector is shown in Figure 12. The ripple counter is clocked by Slow CLK, and increments its count by one each clock cycle. At each stage, the 7-bit comparator compares each count bit to the corresponding bit in the control signal, and outputs a 0 for each equal bit. When the zero-detector detects equivalence in all of the 7 bits, indicating that the desired count has been reached, F_{out} is driven high. On the next clock cycle, the program counter is reset to zero and the count is re-started. In addition, the output pulse on F_{out} is used to reset the count of the swallow counter, indicating the end of one complete cycle of the frequency divider. The ripple counter is implemented using 7 cascaded D-type flip-flops, each arranged in a toggle configuration. The output of each flip-flop is used to clock the next flip-flop. Since the output of each flip-flop inverts on every clock cycle, each flip-flop essentially divides its clock by two, causing the next stage of the ripple counter to be clocked at half the rate of the previous flip flop. Each flip-flop was designed to respond to the falling edge of its clock, when the output of the

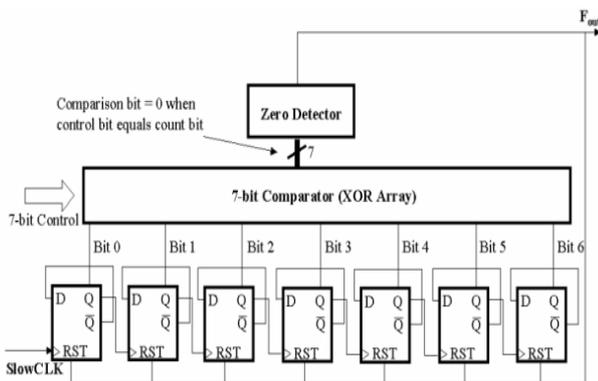


Fig. 5: Block Diagram of a 7-bit Program Counter

Previous stage changes from a 1 to a 0. In this way, an incrementing binary count is achieved with the outputs of each flip-flop forming the bits of the count. Since the program counter contains 7-bits, any count between 0 and 127 can be set by the control signal. It is important to realize however that in order to achieve a division ratio as specified

in the equation $DIV=NP+S$, the control signal must be set to $P-1$, since the zero-state is included in the count.

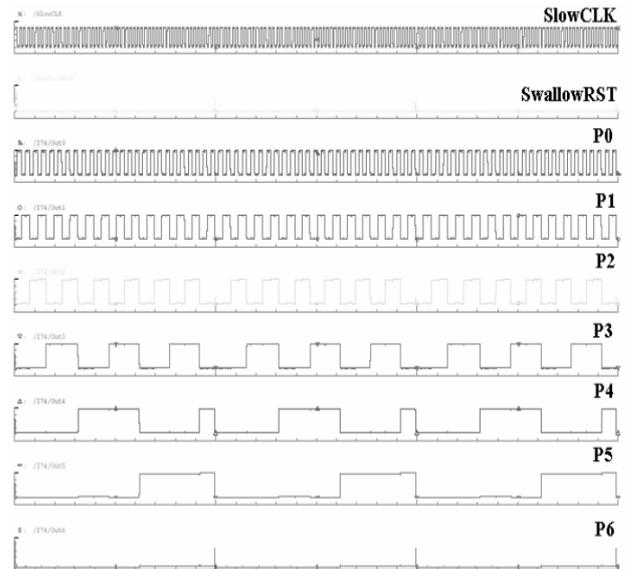


Fig. 6: Program Counter Simulation Results

B. Swallow Counter

The swallow counter, as indicated in Figure 1, is used to count S pulses of Slow CLK before asserting the modulus control signal and changing the modulus of the DMP to N . A block diagram of the swallow counter is provided in Figure 7.

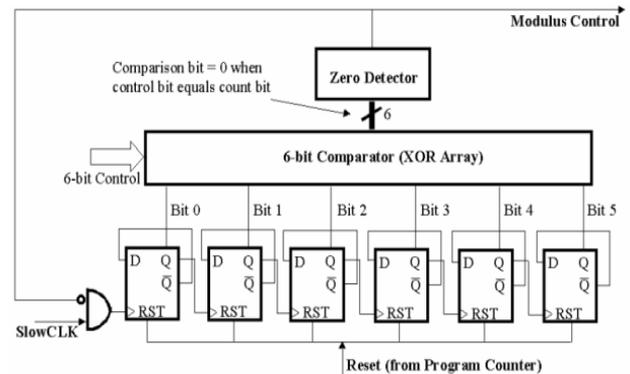


Fig. 7: Block Diagram of a 6-Bit Swallow Counter

By looking at Figure 7, the similarities between the swallow counter and the program counter are apparent. Once again, the count (6-bits in this case) is maintained using a ripple counter comprised of cascaded flip-flops clocked with Slow CLK. In addition, a comparator compares each count bit with its corresponding bit in the control signal, and a zero-detector asserts modulus control when all bits are equal. However, the swallow counter does not reset when the count is reached, but masks the input clock using an AND gate connected to the inverse of modulus control. As a result, the ripple counter stops counting when the count is reached, and the state of the circuit is maintained until a reset signal (Swallow RST) is received from the program counter. Since the swallow counter contains 6 bits, it is capable of any count from 0 to 64. Once again, the control signal must be set to $S-1$, since the zero-state is included in the count.

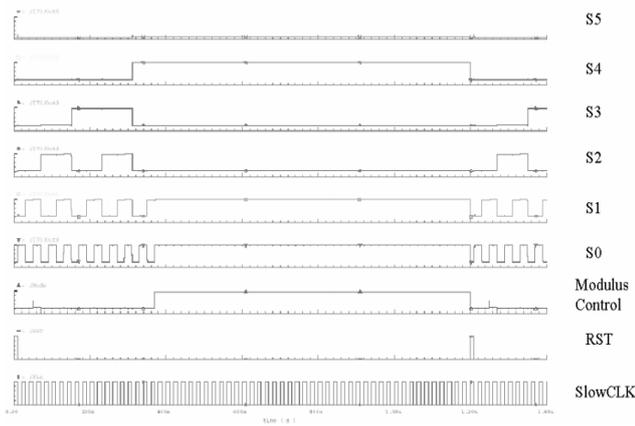


Fig. 8: Swallow Counter Simulation Results (S=20)

VI. SIMULATIONS

The simulations of the designs are performed using MOIDELSIM 6.4b. The simulation results show that the wide band 2/3 prescaler has the maximum operating frequency of 8 GHz with a power consumption of 0.92 and 1.73mW during the divide-by-2 and divide-by-3 modes, respectively. The pro-posed wide band multimodulus prescaler has the maximum operating frequency of 7.2 GHz (simulation) with power consumption of 1.52, 1.60, 2.10, and 2.13mW during the divide-by-32, divide-by-33, divide-by-47 and divide-by-48, respectively. For silicon verification, the multiband divider is fabricated using the Global Foundries 1P6M 0.18- μ m CMOS process On-wafer measurements are carried out using an 8 inch RF probe station. The input signal for the measurement is provided by the 83650B 10 MHz-50 GHz HP signal generator and the output signals are captured by the Lecroy Wave master 8600A 6G oscilloscope. The measurement results shows that the wideband 2/3 prescaler has a maximum operating frequency of 6.5 GHz [10] and the multimodulus 32/33/47/48 prescaler designed using wideband 2/3 prescaler has a maximum operating frequency of 6.2 GHz. However, the maximum operating frequency that can be achieved by the multimodulus 32/33/47/48 prescaler is limited by the wideband 2/3 prescaler. Table I shows the performance of proposed 2/3 prescaler and prescalers reported in [6] and [12] (re simulated). The performance of the multiband flexible divider is measured in both the lower frequency and higher frequency bands by programming the P - and S -counters. Fig. 9 shows the measured output waveform of the multiband divider at an input frequency of 2.47 GHz where P, S -counters are programmed to have values 77 and 6 respectively (FD=2470) Fig. 10 shows the measured output waveform of the multiband divider at an input frequency of 5.818 GHz where P, S -counters are programmed to have values 122 and 38, respectively (FD=5818) The proposed multiband flexible divider consumes an average power of 0.96mW during lower frequency band (2.4–2.484GHz),

While it consumes 2.2mW during the high-frequency band (5–5.825 GHz) of operation compared to the dual-band divider re-ported in [9], which consumes 2.7mW at 1-V power supply. The proposed multiband divider has a variable resolution of K MHz for lower frequency band

(2.4–2.484 GHz) and for the higher frequency band (5–5.825 GHz), where K is integer from 1 to 5 for 2.4-GHz band and 5, 10, and 20 for WLAN applications. Table 1 shows the performance of different dividers.

Design Parameters	[6]	[12]	This work
Process (μ m)	0.18	0.18	0.18
supply voltage (V)	1.8	1.8	1.8
Max.Frequency (GHz) (Sim/Measured)	6.7 / -	7.5 / 6	8 / 6.5
Power(mW) (sim/measured) Divide-by-2 mode	1.88 / -	1.63 / 2.2	0.82 / 0.97
Power(mW) (sim/measured) Divide-by-3 mode	2.18 / -	1.85 / 2.62	1.61 / 1.78

Table. 1: Performance of different 2/3 Prescalers at 2.5 GHz

VII. CONCLUSION

In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer-divider is designed which uses the wideband 2/3 prescaler [17], multimodulus 32/33/47/48 prescaler, and is silicon verified using the 0.18 μ m CMOS technology. Since the multimodulus 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz, the values of P- and S-counters can actually be programmed to divide over the whole range of frequencies from 1 to 6.2 GHz with finest resolution of 1 MHz and variable channel spacing. However, since interest lies in the 2.4- and 5–5.825-GHz bands of operation, the P- and S-counters are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow S-counter and consumes a power of 0.96 and 2.2mW in 2.4- and 5-GHz bands, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing.

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