

Implementation and Performance Analysis of a Vedic Multiplier Using Tanner EDA Tool

Dheeraj Jain¹ Dr. Ajay Somkuwar²

¹Research Scholar ²Professor

¹Dr. K. N. Modi University, Newai , Tonk (Raj.) ²MANIT, Bhopal (M.P.)

Abstract -- high density, VLSI chips have led to rapid and innovative development in low power design during the recent years .The need for low power design is becoming a major issue in high performance digital systems such as microprocessor, digital signal processor and other applications. For these applications, Multiplier is the major core block. Based on the Multiplier design, an efficient processor is designed. Power and area efficient multiplier using CMOS logic circuits for applications in various digital signal processors is designed. This multiplier is implemented using Vedic multiplication algorithms mainly the "UrdhvaTiryakBhyam sutra", which is the most generalized one Vedic multiplication algorithm [1] . A multiplier is a very important element in almost all the processors and contributes substantially to the total power consumption of the system. The novel point is the efficient use of Vedic algorithm (sutras) that reduces the number of computational steps considerably compared with any conventional method . The schematic for this multiplier is designed using TANNER TOOL. Paper presents a systematic design methodology for this improved performance digital multiplier based on Vedic mathematics.

Keywords: Multiplier, Vedic algorithms, Vedic Mathematics, Tanner EDA, UrdhvaTiryakBhyam sutra.

I. INTRODUCTION:

A Multiplier, no doubt, is one of the most important block in any processor now a days. A binary multiplier is an electronic circuit used in digital electronics, such as a computer, to multiply two binary numbers. A variety of computer arithmetic techniques can be used to implement a digital multiplier. Most techniques involve computing a set of partial products, and then summing the partial products together [2]. In the past, the parameters like high speed, small area and low cost were the major areas of concern, whereas power considerations are now gaining the attention of the scientific community associated with VLSI design [3]. In the absence of low-power design techniques such applications generally suffer from very short battery life, while packaging and cooling them would be very difficult and this is leading to an unavoidable increase in the cost of the product. In multiplication, reliability is strongly affected by power consumption. Usually, high power dissipation implies high temperature operation, which, in turn, has a tendency to induce several failure mechanisms in the system. Power dissipation is the most critical parameter for portability & mobility and it is classified in to dynamic and static power dissipation.

As the common digital signal processing algorithms spend most of their time multiplying, the processors spend a lot of chip area in order to make the multiplication as fast as

possible. Hence a non-conventional yet very efficient Vedic mathematics is used for making a high performance multiplier. Vedic Mathematics deals mainly with various Vedic mathematical formulae and their applications for carrying out large arithmetical operations easily [4].

This paper is based on UrdhvaTiryakBhyam sutra of Vedic multiplication, which is the most generalized method for multiplication. Considering a digital hardware, a Vedic multiplier will be more power efficient and faster also as less number of steps are required for multiplication

II. URDHVA-TIRYAKBHYAM SUTRA MULTIPLICATION:

Urdhva Tiryakbhyam Sutra from Vedic mathematics is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products

In this paper, comparative study of different multipliers is done for low power requirement and high speed.

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (325 * 738). Line diagram for the multiplication is shown in Fig.1. Initially the LSB digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and the process goes on likewise. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit act as the result digit and all other digits act as carry for the next step. Initially the carry is taken to be zero.

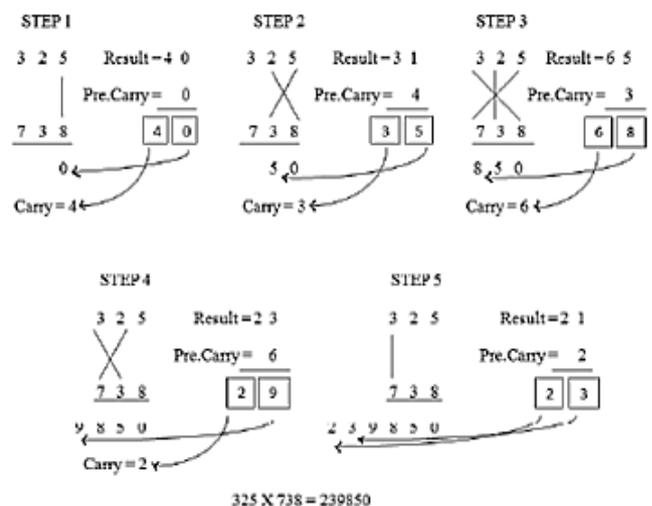


Fig. 1: Multiplication of two numbers using Urdhva Tiryakbhyam Sutra

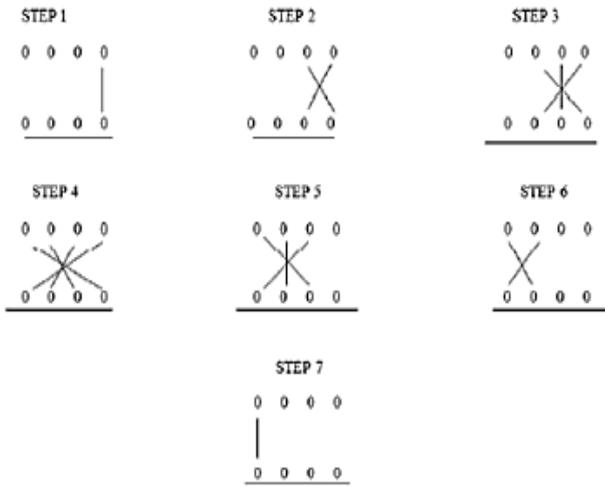


Fig. 2: Line diagram of the multiplication

III. VLSI TECHNOLOGY USING CMOS LOGIC

Large integrated circuits can be constructed using CMOS logic with very low static power consumption. The increasing demand for low power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation—switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important. In the past, the parameters like high speed, small area and low cost were the major areas of concern, whereas power considerations are now gaining the Attention of the scientific community associated with VLSI design. In recent years, the growth of Personal computing devices (portable computers and real time audio and video based multimedia applications) and wireless communication systems has made power dissipation a most critical design parameter [5]. In the absence of low-power design techniques such applications generally suffer from very short battery life, while packaging and cooling them would be very difficult and this is leading to an unavoidable increase in the cost of the product.

In multiplication, reliability is strongly affected by power consumption. Usually, high power dissipation implies high temperature operation, which, in turn, has a tendency to induce several failure mechanisms in the system [6]. Power dissipation is the most critical parameter for portability & mobility and it is classified in to dynamic and static power dissipation. Dynamic power dissipation occurs when the circuit is operational, while static power dissipation becomes an issue whether circuit is inactive or is in a power-down mode. There are three major sources of power dissipation in digital CMOS circuit which are summarized in equation (1)

$$P_{avg} = P_{switching} + P_{short\ circuit} + P_{leakage} \quad (1)$$

IV. 8-BIT VEDIC MULTIPLIER:

An 8-bit VEDIC multiplier is made using four, 4 bit Vedic multipliers and three, 16 bit adders. The design is then simulated in Tanner tool. The smallest sub-circuit instance being used here is of a Full adder. The systematic design flow then includes a 4-bit Vedic multiplier and finally the 8-bit Vedic multiplier.

Part 1: A 14 -T full-adder cell [7]

The full adder being used here is a 14 transistor adder based on complementary pass-transistor logic (CPL) [11]. The general structure of the 14 transistor adder is shown in the Fig 3(a) below. It is composed of XOR/XNOR gate instances combined together to make a low power full-adder cell with high node voltage swings [7],[8]. The sum and carry (Cout) outputs are generated from the binary inputs A, B, Cin and expressed as

$$\text{Sum} = A \text{ XOR } B \text{ XOR } C_{in} \quad (2)$$

$$\text{Cout} = A \cdot B + C_{in} \cdot (A \text{ XOR } B) \quad (3)$$

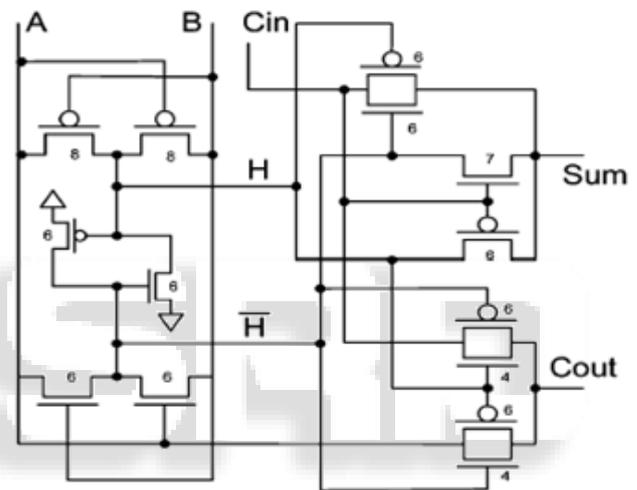


Fig. 3: 14-T cell using CMOS logic

A. Simulation in tanner tool

Fig. 3 and Fig. 4 below shows the respective schematic and simulation results on Tanner. The simulation result of the full-adder cell is shown in the Fig. 3(c) below.

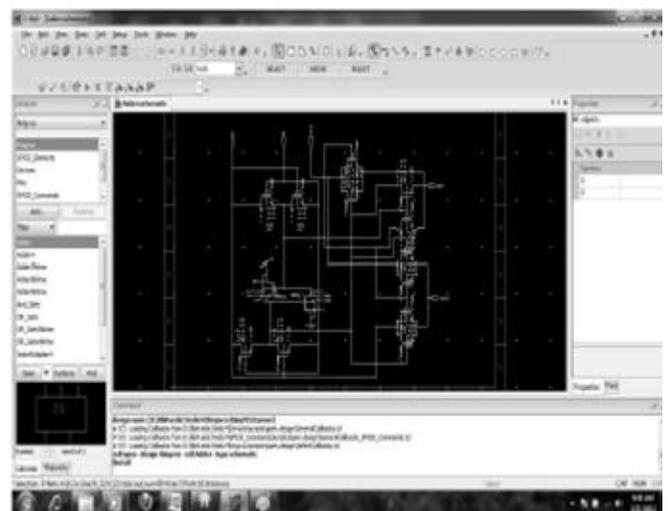


Fig. 4: Schematic for 14 transistor full-adder in tanner tool.

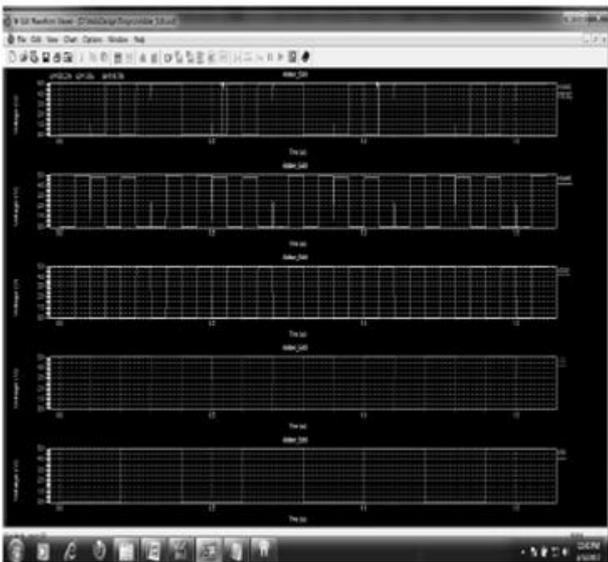


Fig. 5: Input stimulus for a full-adder cell. The bottoms there are inputs A, B, and Cin and the remaining two are outputs (Cout and Sum)

Part 2:- 4-bit multiplier

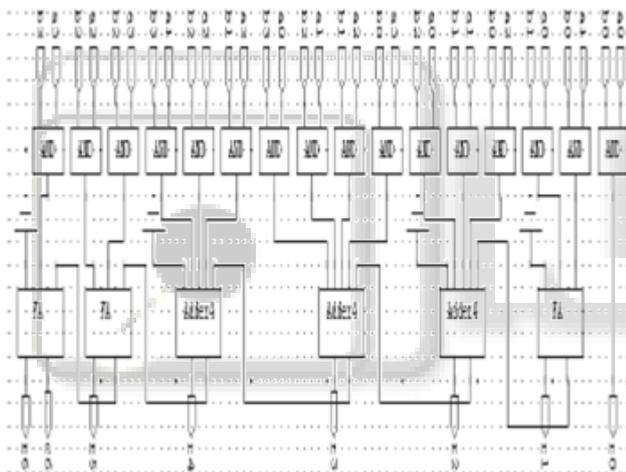


Fig. 6: Schematic design for the 8-bit Vedic multiplier

B. Simulation in tanner tool

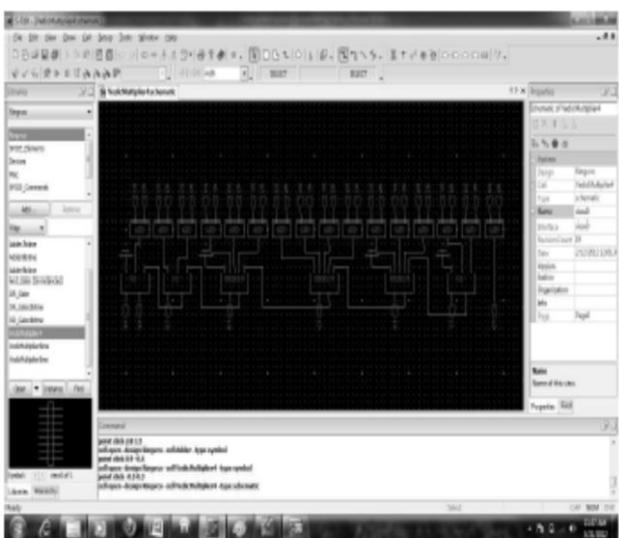


Fig. 7: Schematic for 4-bit Vedic multiplier in tanner tool

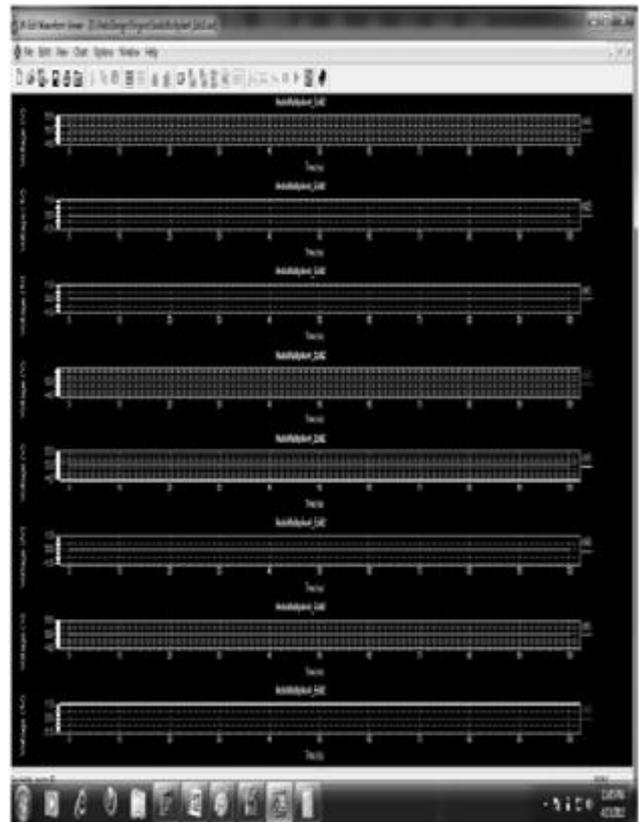


Fig. 8: Input values for multiplier as VA= 1001 & VB=1010
The 4-bit Vedic multiplier design using adders and gate instances is shown in the figure 3(a) above. Two 4-bit inputs VA and VB are multiplied here. The first input is a3a2a1a0 and second b3b2b1b0. All the instances used here are made using CMOS logic.

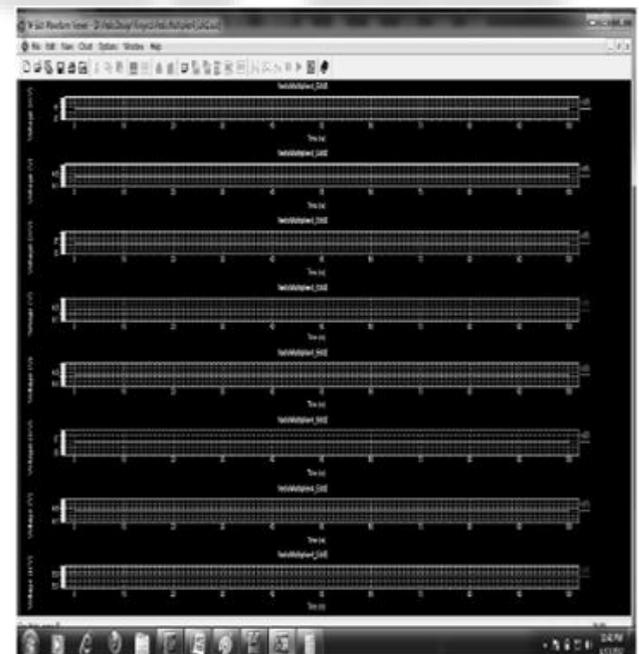


Fig. 9: Output value of the multiplier, 01011010
Part 3:- 8-bit digital Vedic multiplier using four, 4-bit multipliers
Now using the results of the 4-bit Vedic multiplier obtained above A 8-bit multiplier is designed.

In this 8-bit multiplier the 8-bit input is divided into two halves of 4 bit each [9].

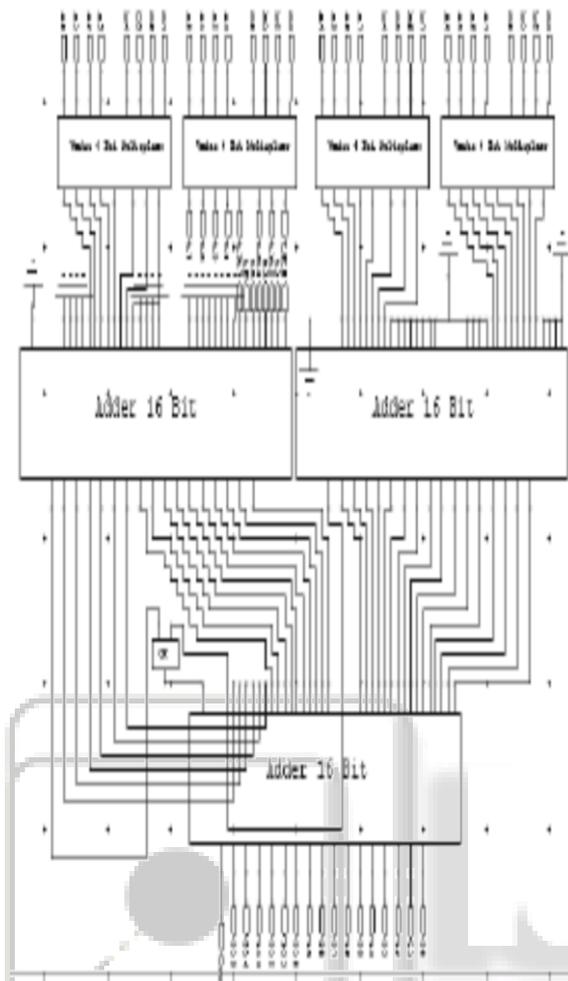


Fig. 10: Schematic design for the 8-bit Vedic multiplier

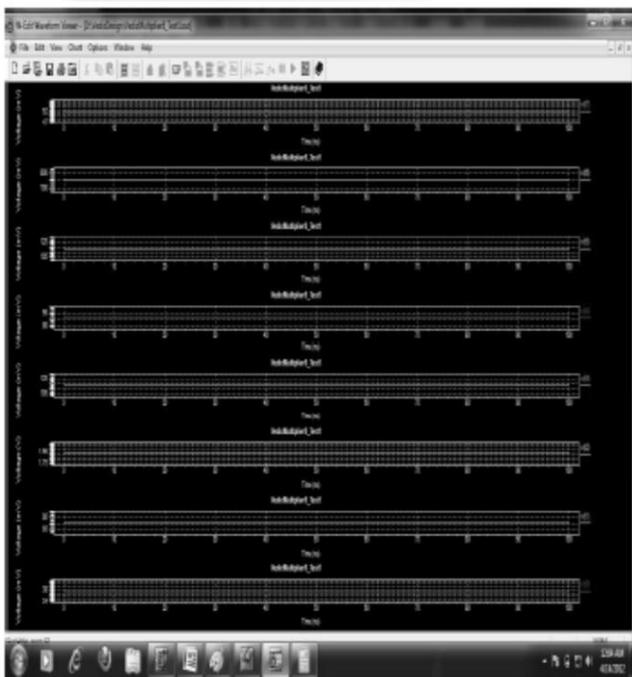


Fig. 11: output value of the multiplication obtained after Random input values

V. SIMULATION RESULT ANALYSIS:

The multiplier blocks are simulated using T-SPICE netlist and the results are verified for both the 4-bit and 8-bit multiplier.

1. For the 4-bit Vedic multiplier:
Measurement result summary
avgpower = 1.4714e-002 W
Core Area = 110 um²
Processor time required = 5.43 Seconds
2. For the 8-bit Vedic multiplier:
Measurement result summary
avgpower = 10.3868e-002 W
Core Area = 740 um²
Processor time required = 15.23 Seconds

Both for a transition time of 100ns.

When compared with the results obtained in [10], the power consumption and processor time required is found to be very less. The power consumption using the gate level analysis in [10] for a 4-bit multiplier is found to be 0.55W whether the results obtained in this paper using transistor level analysis , gives it to be around 11 mW . The power consumption for the 8-bit multiplier structure here using four , 4-bit multipliers is found to be around 89 mW The processor time required in the gate level analysis in [10] is 7.40 Seconds for the 4-bit multiplier against the 5.43 seconds obtained in the Vedic multiplier designed above using CMOS VLSI technology. Again the computational steps are also reduced and hardware implementation required will also be less as compared to the conventional methods and hence enhancing the performance of the overall system.

VI. CONCLUSION:

This paper represents a efficient Vedic multiplier design using VLSI technology. Almost 80% power reduction at 2.5 volts can be achieved using this Vedic multiplier as compared to its earlier counterparts using gate level analysis or the conventional ways of multiplication. The processor's time consumption is reduced from 7.40 Seconds to 5.43 Seconds for the 4-bit Vedic multiplier and the computational complexity is also less as it is requiring less number of steps as compared to conventional multiplication methods. For a real world application of this multiplier, it is implemented for finding out the determinant of a 2 X 2 matrix which will be having two, 8-bit multipliers and finding the difference of both using two's compliment.

VII. REFERENCES:

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