Design of Low Power, High Speed 3-Bit Pipelined ADC

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Abstract— The design of high speed, lower power A/D converter architectures have been investigated and can be found in several applications. The low power techniques used in this design include the dynamic comparators and capacitor scaling which are made possible with this architectural selection. To be compatible with the digital integrated circuit now running at 3.3V power supply, some techniques for low supply voltage are introduced, which include a 3.3V Op Amp and low voltage SC circuits.

In order to reduce the power even more, one can reduce the per-stage resolution and cascade more stages to get the full resolution. This particular architecture is called the Pipelined architecture, mainly because the analog input signal is passed through a pipeline of flash A/D (sub-ADC) and interstate gain blocks. The advantage of this architecture is its reduced complexity. With a given per-stage resolution, an A/D converter of a given resolution can be achieved by cascading an appropriate number of identical pipelined stages. In any A/D converters, some reference voltages are generally required to set a reference for the sampled input to be compared to.

Tspice simulation results & Layout using 1.2µm CMOS Technology parameters for the proposed design of Low Power – Low Voltage 3 bit Pipelined ADC are discussed.

Keyword--Sample & Hold, Comparator, Buffer, Reference Voltage Generator, Subtractor cum amplifier, Switch

I. INTRODUCTION

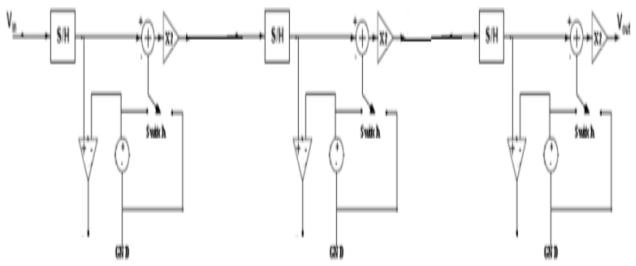


Fig. 1: Pipeline ADC

Pipelined ADC: In order to reduce the power even more, one can reduce the per-stage resolution and cascade more stages to get the full resolution. Such architecture is called the Pipelined architecture, mainly because the analog input signal is passed through a pipeline of flash A/D (sub-ADC) and interstate gain blocks. The analog input signal is sampled by a S/H circuit. The sampled input signal is then converted to the resolution of the stage, B bits; concurrently is also subtracted from the DAC output of the present stage digital output. The residue is then amplified by the factor 2B and passed down to the next stage. Identical operation is performed for each stage and the digital outputs are combined properly to achieve the required MxB bit full A/D resolution.

The advantage of this architecture is its reduced complexity. With a given per-stage resolution, an A/D converter of a given resolution can be achieved by cascading an appropriate number of identical pipelined stages. The major disadvantage of this architecture is the latency in the converter. Generally, if concurrent or interleaving processing is used, the delay through the converter is roughly clock cycles.

A. Power-Optimized Pipelined A/D Architecture:

In the conventional pipelined A/D architecture, the trade-off between the per-stage resolution and power is tradeoff. For a given sampling rate, when increasing the per-stage resolution, the required number of stages is reduced; however each stage will require more power because of multiple bits. When decreasing the per-stage resolution, the required number of stages is increased; however each stage will require less power. Below is an attempt to estimate the power for the conventional pipelined A/D architecture with different per-stage resolution.

Using the conventional pipelined A/D converter, each stage is identical and performs the same functionality. The power comparison can be found by comparing the power per stage and multiply by the number of stages, a stage in the pipeline loaded by the next stage. The total number of stages is roughly the full resolution of the converter divided by B, per-stage resolution. And the number of comparator required in each stage is about the low-power techniques include the choice of per-stage resolution, capacitor scaling and digital correction. It has been found for high conversion rate, a low per-stage resolution (hence low closed loop gain) is more desirable. With capacitor scaling and digital correction, each stage in the pipeline can be designed according to the noise limitation, hence reduce power dissipation. With the above techniques, a CMOS implementation of such a power-optimized pipelined A/D converter will be presented.

II. SAMPLE & HOLD

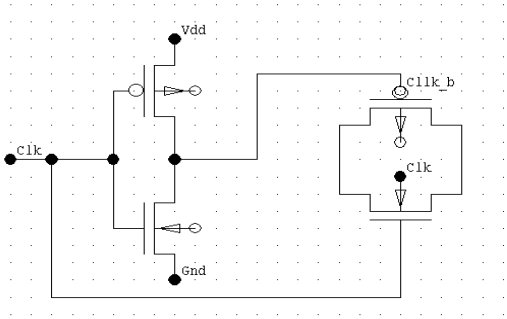


Fig. 2: Sample & Hold

Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. The simplest S/H circuit in which Vin is the input signal, *M1* is an MOS transistor operating as the sampling switch, *Ch* is the hold capacitor, *ck* is the clock signal, and *Vout* is the resulting sample-and-hold output signal.

A S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever *ck* is high, the MOS switch is on, which in turn allows *Vout* to track *Vin*. When *ck* is low, the MOS switch is off. During this time, *Ch* will keep *Vout* equal to the value of *VIN* at the instance when *ck* goes low.

III. COMPARATOR

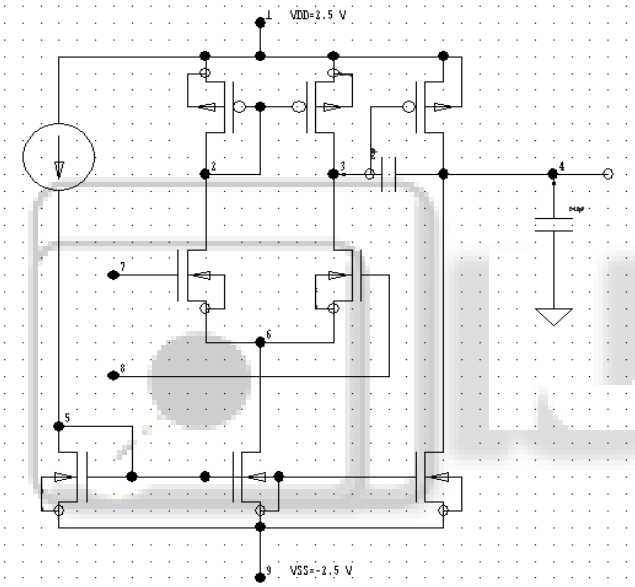
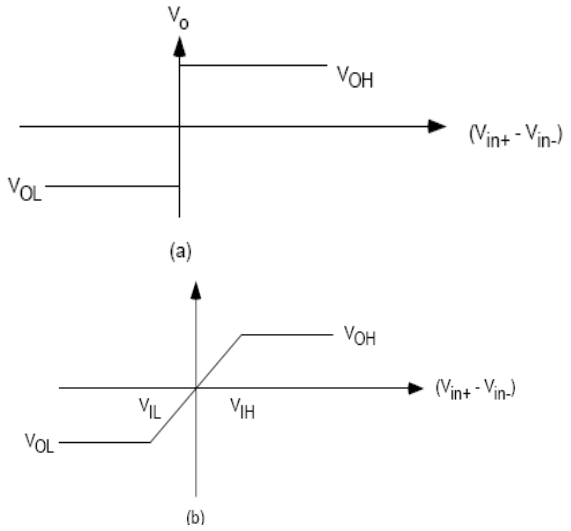
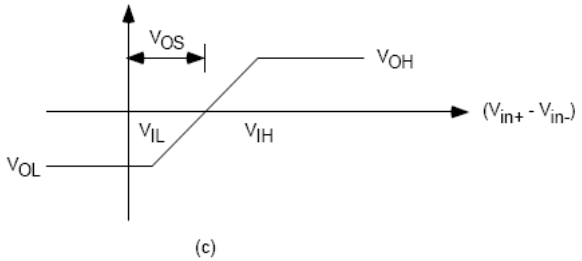


Fig. 3: Comparator





A comparator is a circuit that has binary output.
Ideally its output shown in Figure is defined as follows:

$$V_o = \begin{cases} V_{OH} & \text{if } V_{in+} - V_{in-} > 0 \\ V_{OL} & \text{if } V_{in+} - V_{in-} < 0 \end{cases}$$

This is not realizable because its gain is infinity. It shows a realizable first order transfer characteristic of a comparator. Its output is defined as follows:

$$V_o = \begin{cases} V_{OH} & \text{if } (V_{in+} - V_{in-}) > V_{IH} \\ A_V(V_{in+} - V_{in-}) & \text{if } V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & \text{if } (V_{in+} - V_{in-}) < V_{IL} \end{cases}$$

Another non ideal characteristic of practical comparator is the present of input offset. That is the output does not change until the input difference reached the input offset Vos. It shows this transfer characteristic. Its output is defined as follows:

$$V_o = \begin{cases} V_{OH} & \text{if } (V_{in+} - V_{in-}) > V_{IH} \\ A_V(V_{in+} - V_{in-}) - A_V V_{OS} & \text{if } V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & \text{if } (V_{in+} - V_{in-}) < V_{IL} \end{cases}$$

If the input step is sufficiently small the output should not slew and the transient response will be a linear response. The settling time is the time needed for the output to reach a final value within a predetermined tolerance, when excited by a small signal. Small-signal settling time is determined by the gain bandwidth product of the amplifier, this will be shown in the OpAmp circuit section later. If the input step magnitude is sufficiently large, the comparator will slew by virtue of not having enough current to charge or discharge the compensating and/or load capacitances. The slew rate is determined from the slope of the output waveform during the rise or fall of the output. Slew rate is limited by the current-sourcing/sinking capability in charging the output capacitor.

Settling time is important in analog signal processing. It is necessary to wait until the amplifier has settled to within a few tenths of a percent of its final value in order to avoid errors in the accuracy of processing analog signals. A longer settling time implies that the rate of processing analog signals must be reduced.

IV. REFERENCE VOLTAGE GENERATOR

In any A/D converters, some reference voltages are generally required to set a reference for the sampled input to be compared to. The accuracy of the reference voltages need

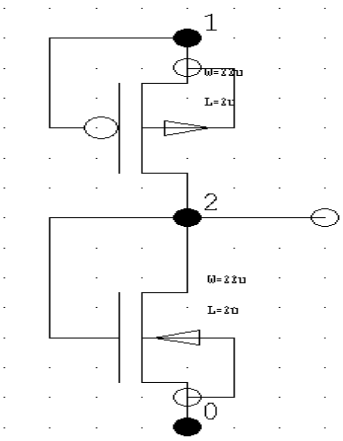


Fig. 4: Ref. Voltage Generator

to be as linear as the converter itself in most cases. For example, in flash converters, reference voltages are compared with the sampled input signal. Any error present on reference voltages will be added directly to the nonlinearity of the converter. The problem becomes even more severe at high resolution and high speed. In a high speed converter, switching noise on the chip can be coupled onto the reference lines and corrupt the conversion process. Traditionally, there are two ways to generate reference voltages either by using a resistor string or capacitor array. Each one has its own limitations. The number of required voltage references has been reduced to two and the tolerance is relaxed with some trimming capacitor.

A. BUFFER

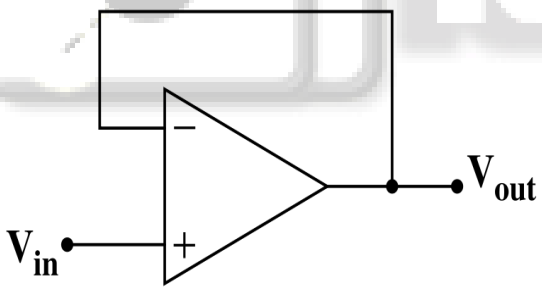


Fig. 5: Buffer

A buffer amplifier (sometimes called a buffer) is one that provides electrical impedance transformation from one circuit to another.

Typically a buffer amplifier is used to transfer a voltage from a first circuit, having a high output impedance level, to a second circuit with a low input impedance level. The interposed buffer amplifier level to a second circuit with s low input impedance level. The interposed buffer amplifier prevents the second circuit from loading the first circuit unacceptably and interfering with its desired operation.

If the voltage is transferred unchanged (the voltage gain is 1), the amplifier is a unity gain buffer, also known as a voltage follower.

Although the voltage gain of a buffer amplifier may be (approximately) unity, it usually provides considerable current gain and thus power gain. However, it is commonplace to say that is has a gain of1 (or the equivalent 0 dB), referring to the voltage gain.

B. SWITCH

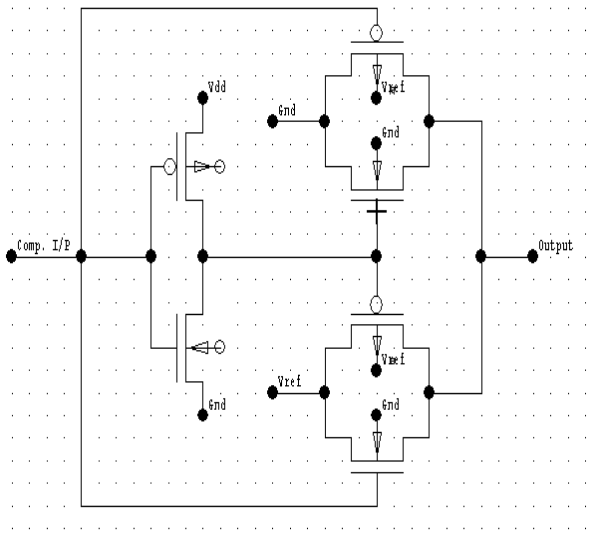


Fig. 6: Switch

In recent years, integrated analog switches have offered better switching characteristics, lower supply voltages, and smaller packages. Because so many performance options and special functions are available, the well-informed product designer can usually find the right part for a particular application.

CMOS analog switches are easy to use, so most designers take them for granted. But one should not forget that these switches solve specific engineering problems

Connecting an n-channel MOSFET in parallel with a p-channel MOSFET allows signals to pass in either direction with equal ease. Whether the n- or the p-channel device carries more signal current depends on the ratio of input to output voltage. Because the switch has no preferred direction for current flow, it has no preferred input or output. The two MOSFETs are switched on and off by internal inverting and non inverting amplifiers. These amplifiers level-shift the digital input signal as required, according to whether the signal is CMOS- or TTL-logic-compatible and whether the analog supply voltage is single or dual.

C. SUBTRACTOR CUM AMPLIGIER

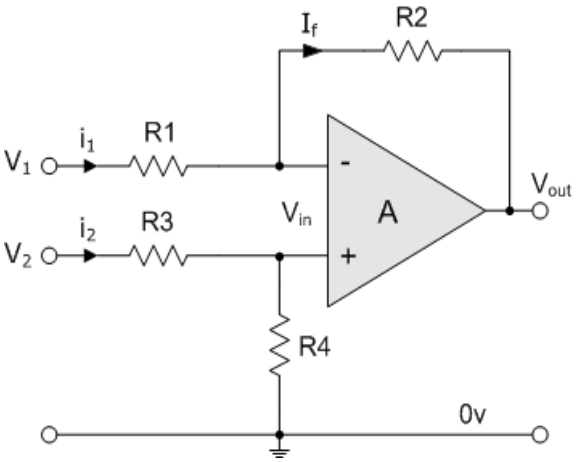


Fig. 7: Subtractor cum Amplifier

The MOSFET Operational amplifier is one of the most important circuits used in analogue design. This tutorial will discuss the basic features of a two-stage op-amp, define the equations required to meet specific design goals and most important of all the frequency response and stability of op-amps. The basic MOS two-stage compensated OP-AMP – using a capacitive load. M6 sets the 'tail' current and by mirroring the bias current to the output stage. M3 and M4 form the differential amplifier Note P-type devices have been used as these have better noise performance. M5 is the current source for the differential amplifier and has been initially set at 30uA. The current mirror formed by M1 and M2 'combine' the differential output voltage to give a single voltage output feeding into M8. M8 is a simple current source inverter with miller compensating capacitor Cc.

The input features of the op-amp are based on the differential amplifier with high impedance inputs. The output stage has a low impedance output and the total gain of the op-amp is the product of the two individual stage gains. As the output impedances of each stage are similar (ie RO1 ~ RO2) then without compensation the frequency poles caused by the interaction of C1.RO1 and C2.RO2 are at similar frequencies resulting in poor phase margin. To split the poles (i.e move them further apart) we introduce the miller capacitor (Cc) to ensure a lower frequency dominant pole formed by Cc.RO1.RO2. The addition of the miller compensation capacitor Cc introduces a high frequency zero that will degrade the phase margin and peak up the gain so efforts have to be made to increase the frequency of the zero or eliminate it all together.

V. DESIGN SPECIFICATION

Technology	1.2µm CMOS Technology
Supply Voltage	2.5 V
Resolution	3 bits
Input Voltage Range	2.5 Vp-p
DNL	<0.5 LSB
INL	<0.5 LSB
Power Dissipation	Appx. 40mW
Active Area	0.46mm^2
Input Frequency	200 KHz
Slew Rate	100V/us

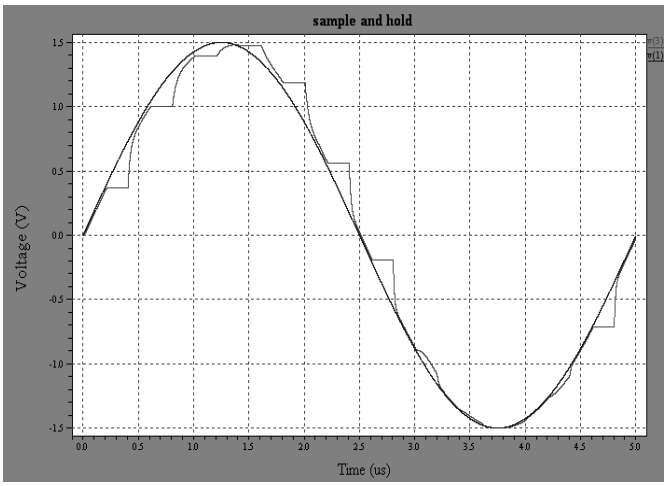
Table (1): design specification

VI. OBSERVATION TABLE

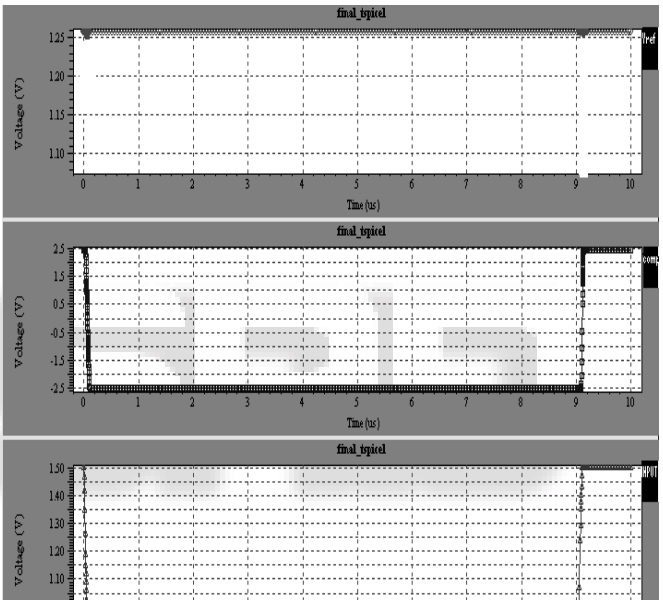
Observations Table											
First stage				Second stage				Third stage			
I/P	Comp.	Sub.	Amp.	I/P	Comp.	Sub.	Amp.	I/P	Comp.	Sub.	Amp.
0.3125	0	0.3125	0.625	0.625	0	0.625	1.25	1.25	0	1.25	2.5
0.625	0	0.625	1.25	1.25	0	1.25	2.5	2.5	1	1.25	2.5
0.9375	0	0.9375	1.875	1.875	1	0.625	1.25	1.25	0	1.25	2.5
1.25	0	1.25	2.50	2.5	1	1.25	2.5	2.5	1	1.25	2.5
1.5625	1	0.3125	0.625	0.625	0	0.625	1.25	1.25	0	1.25	2.5
1.875	1	0.625	1.25	1.25	0	1.25	2.5	2.5	1	1.25	2.5
2.1875	1	0.9375	1.875	1.875	1	0.625	1.25	1.25	0	1.25	2.5
2.5	1	1.25	2.5	2.5	1	1.25	2.5	2.5	1	1.25	2.5

Table (2): Observation Table

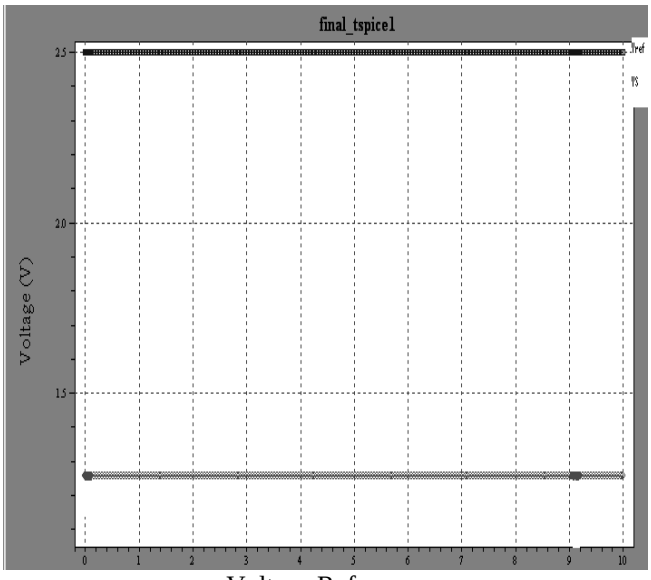
VII. SIMULATION RESULTS



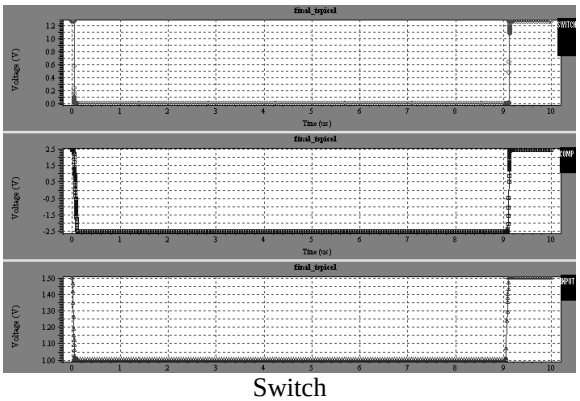
Sample & Hold Circuit



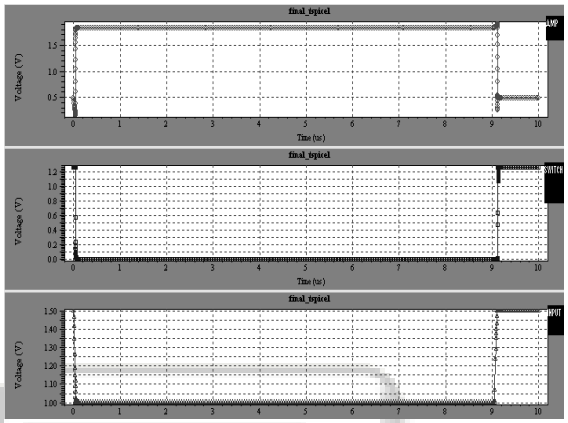
Comparator



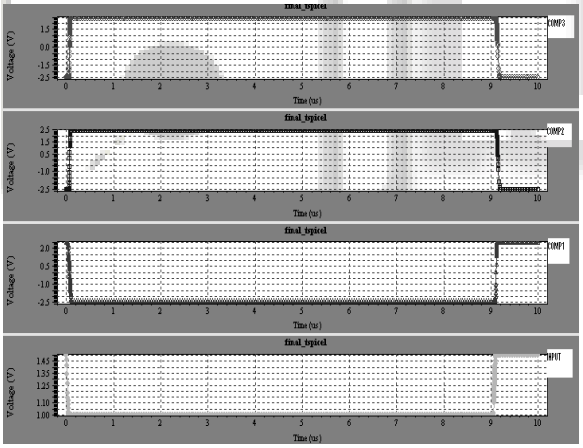
Voltage Reference



Switch



Subtractor cum Amplifier



Final Output waveforms

VIII. CONCLUSION

A high speed, low power and low voltage A/D converter with scaled technology has been investigated here.

In circuit level, taking advantage of digital correction, dynamic comparators are used to eliminate static power consumption. The pipelined ADC is the architecture of choice for sampling rates from a few Msps up to 100Msps+.

Pipelined ADCs are very useful for a wide range of applications, most notably in digital communication where a converter's dynamic performance is often more important than traditional DC specifications like differential nonlinearity (DNL) and integral nonlinearity (INL).

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