Introduction to VIP with PCI Express Technology

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Abstract—This paper describes latest technology PCI Express and VIP for reusability purpose as it is necessary for today’s faster verification needs. It is explained using PCIe Verification IP. This verification is achieved by developing Device reference module. PCIe is high speed serial bus that supports 2.5 GT/s to 16 GT/s. PCIe is point to point device with lane and link concept that support full duplex communications between two devices. Verification Intellectual Property is component that behaves exactly like PCIe design and used for verification of the design. Additionally it has several features like generation, checking and coverage. PCIe VIP is architecture using system Verilog HVL.

Keywords—ASIC, TL, DLL, Lane, Link, Verification, VIP (Verification Intellectual Property)

I. INTRODUCTION
PCI Express (PCIe) is the third generation, general purpose and high performance I/O bus used to interconnect peripheral devices to a computer. PCI Express architecture is a high performance, IO interconnect for peripherals in computing/communication platforms Evolved from PCI and PCI-X architectures Yet PCI Express architecture is significantly different from its predecessors PCI and PCI-X.

Fig. 1: PCI Express Link

Here the idea is to develop a Verification IP for PCI Express. Verification IP are reusable verification modules that typically consist of bus functional models, traffic generators, protocol monitors, and functional coverage blocks. Each of the verification IP (VIP) accelerates the development of a complete verification environment to cut down the time to first test.

Based on widely used and emerging protocols, verification IP are standards-compliant, plug and play modules that cut down overall verification time for engineers using different HVL. They contain the necessary infrastructure for test-bench generation and checking mechanisms, as well as all the appropriate routines to create individual protocols or bus functional models.

Verification IP solutions enable verification engineers to focus on verifying their designs rather than spending an excessive amount of time setting up complex verification environments.

II. ARCHITECTURE

A. Root Complex:
Root Complex (RC) is the root of an I/O hierarchy and it connects the CPU or memory subsystem to the I/O devices.

It is shown in Fig 2 that a Root Complex may support one or more PCI Express Ports. Each interface defines a separate hierarchy domain. Each hierarchy domain may be composed of a single Endpoint or a sub-hierarchy containing one or more Switch components and Endpoints.

The capability to route peer-to-peer transactions between hierarchy domains through a Root Complex is optional and implementation dependent. For example, an implementation may incorporate a real or virtual Switch internally within the Root Complex to enable full peer-to-peer support in a software transparent way.

B. Endpoints:
Endpoint is a type of Function that can be the Requester or Completer of a PCI Express transaction either itself or on behalf of a distinct non-PCI Express device (something other than a PCI device or Host CPU), e.g., a PCI Express attached graphics controller or a PCI Express-USB host controller. Endpoints are classified as either legacy, PCI Express, or Root Complex Integrated Endpoints.

Packets are transmitted and received serially and byte striped across the available Lanes of the Link. The more Lanes implemented on a Link the faster a packet is transmitted and the greater the bandwidth of the Link.

Fig. 2: Example topology
Below Fig (3) shows all layers of PCIe.

![PCI Express layers](image)

**Fig. 3: PCI Express layers**

III. DEVICE LAYERS AND THEIR ASSOCIATED PACKETS

Three categories of packets are defined; each one is associated with one of the three device layers. Associated with the Transaction Layer is the Transaction Layer Packet (TLP). Associated with the Data Link Layer is the Data Link Layer Packet (DLLP). Associated with the Physical Layer is the Physical Layer Packet (PLP). These packets are introduced next.

A. Transaction Layer Packets (TLPs)

PCI Express transactions employ TLPs which originate at the Transaction Layer of a transmitter device and terminate at the Transaction Layer of a receiver device. This process is represented in Fig 4. The Data Link Layer and Physical Layer also contribute to TLP assembly as the TLP moves through the layers of the transmitting device.

At the other end of the Link where a neighbor receives the TLP, the Physical Layer, Data Link Layer and Transaction Layer disassemble the TLP.

![TLP Origin and Destination](image)

**Fig. 4: TLP Origin and Destination**

1) TLP Packet Assembly

A TLP that is transmitted on the Link appears as shown in Fig 5.

![TLP Assembly](image)

**Fig. 5: TLP Assembly**

The software layer or device core sends information required to assemble the core part of TLP which is header and data portion of the packet to the Transaction Layer.

Some TLPs do not contain a data section. An optional End-to-End CRC (ECRC) field is calculated and appended to the packet. The ECRC field is used by the ultimate targeted device of this packet to check for CRC errors in the header and data portion of the TLP.

![TLP Assembly](image)

**Fig. 6: TLP Assembly**

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The core section of the TLP is forwarded to the Data Link Layer which then appends a sequence ID and another LCRC field. The LCRC field is used by the neighboring receiver device at the other end of the Link to check for CRC errors in the core section of the TLP plus the sequence ID.

The resultant TLP is forwarded to the Physical Layer which concatenates a Start and End framing character of 1 byte each to the packet. The packet is encoded and differentially transmitted on the Link using the available number of Lanes.
2) A.2 TLP Packet Disassembly

A neighboring receiver device receives the incoming TLP bit stream. As shown in Fig 6 the received TLP is decoded by the Physical Layer and the Start and End frame fields are stripped.

The resultant TLP is sent to the Data Link Layer. This layer checks for any errors in the TLP and strips the sequence ID and LCRC field. Assume there are no LCRC errors, then the TLP is forwarded up to the Transaction Layer. If the receiving device is a switch, then the packet is routed from one port of the switch to an egress port based on address information contained in the header portion of the TLP.

The resultant TLP is sent to the Data Link Layer. This layer checks for any errors in the TLP and strips the sequence ID and LCRC field. Assume there are no LCRC errors, then the TLP is forwarded up to the Transaction Layer. If the receiving device is a switch, then the packet is routed from one port of the switch to an egress port based on address information contained in the header portion of the TLP.

The ultimate targeted device of this TLP checks for ECRC errors in the header and data portion of the TLP. The ECRC field is removed, leaving the header and data portion of the packet. It is this information that is finally forwarded to the Device Core/Software Layer.

B. Data Link Layer Packets (DLLPs)

Another PCI Express packet called DLLP originates at the Data Link Layer of a transmitter device and terminates at the Data Link Layer of a receiver device. This process is represented in Fig 7. The Physical Layer also contributes to DLLP assembly and disassembly as the DLLP.

It moves from one device to another via the PCI Express Link.

DLLPs are used for Link Management functions including TLP acknowledgement associated with the ACK/NAK protocol, power management, and exchange of Flow Control information. DLLPs are transferred between Data Link Layers of the two directly connected components on a Link. DLLPs do not pass through switches unlike TLPs which do travel through the PCI Express fabric. DLLPs do not contain routing information. These packets are smaller in size compared to TLPs, 8 bytes to be precise.

1) DLLP Assembly

The DLLP shown in Fig 8 on page 76 originates at the Data Link Layer. There are various types of DLLPs some of which include Flow Control DLLPs (FCx), acknowledge/no acknowledge DLLPs which confirm reception of TLPs (ACK and NAK), and power management DLLPs (PMx). A DLLP type field identifies various types of DLLPs. The Data Link Layer appends a 16-bit CRC used by the receiver of the DLLP to check for CRC errors in the DLLP.

2) DLLP Disassembly

The DLLP is received by Physical Layer of a receiving device. The received bit stream is decoded and the Start and End frame fields are stripped.

The resultant packet is sent to the Data Link Layer. This layer checks for CRC errors and strips the CRC field. The Data Link Layer is the destination layer for DLLPs and it is not forwarded up to the Transaction Layer.

C. Physical Layer Packets (PLPs)

Another PCI Express packet called PLP originates at the Physical Layer of a transmitter device and terminates at the Physical Layer of a receiver device.

Some PLPs are used during the Link Training process. PLPs are used to place a Link into the electrical idle low power state or to wake up a Link from this low power state.

IV. VERIFICATION

A. Importance of VIP:

Advanced verification techniques allow the user to increase the quality and level of verification. New test bench languages support more sophisticated types of testing, such as advanced random testing methods. Coverage tools enable the users to determine the how much verification is done on different parts of the code providing some feedback on the quality.

Fig. 7: TLP Disassembly

Switches are allowed to check for ECRC errors and even report the errors it finds and error. However, a switch is not allowed to modify the ECRC that way the targeted device of this TLP will detect an ECRC error if there is such an error.

The ultimate targeted device of this TLP checks for ECRC errors in the header and data portion of the TLP. The ECRC field is removed, leaving the header and data portion of the packet. It is this information that is finally forwarded to the Device Core/Software Layer.

Fig. 8: DLLP Origin and Destination

The DLLP content along with a 16-bit CRC is forwarded to the Physical Layer which appends a Start and End frame character of 1 byte each to the packet. The packet is encoded and differentially transmitted on the Link using the available number of Lanes.

2) DLLP Disassembly

The DLLP is received by Physical Layer of a receiving device. The received bit stream is decoded and the Start and End frame fields are stripped.

The resultant packet is sent to the Data Link Layer. This layer checks for CRC errors and strips the CRC field. The Data Link Layer is the destination layer for DLLPs and it is not forwarded up to the Transaction Layer.

Fig. 9: DLLP Assembly

The DLLP type field identifies various types of DLLPs. The Data Link Layer appends a 16-bit CRC used by the receiver of the DLLP to check for CRC errors in the DLLP.

Fig. 9: DLLP Assembly
VIP should be developed so as to fully exercise the protocol implemented by standards based IP. One extension of this is the provision of compliance checking VIP from a standards body or technology leader.

The PCI Express (PCIE) Verification IP is a reusable, configurable, pre-verified, plug-and-play verification component developed in System Verilog. It offers an easy to use and complete verification solution for SoCs incorporating PCI Express Endpoints, Root Complex, or Switch at module, chip and system level. The PCI Express VIP supports automatic stimulus generation, assertion checking, protocol checking and functional coverage analysis all within a single, extensible component.

PCIE VIP provides a simple yet powerful user interface which drastically reduces the time and effort needed to create a verification environment and verify thoroughly to ensure first time right silicon. Using random stimulus generation and coverage driven methodology provided in PCIE VIP, user can verify the design with limited test cases in very short duration instead of running large number of directed test cases.

B. Role of VIP:
The role of Verification IP (VIP) in the development and successful usage of complex Semiconductor IP (SIP) cores is tremendous.

The use of standards based verification languages, provides designers access to key analytical functions such as transactions and assertions, which enable the validation of complex functional behavior. It is important to have testing methods for the verification IP to demonstrate the quality and the interoperability with Other parts of the verification environment.

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REFERENCES