# Simulation of 3 bit Flash ADC in 0.18µmTechnology using NG SPICE Tool for High speed Application

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*Abstract*— This paper provides the basic simulation result for the 3 bit flash type ADC in 0.18µm technology using the NG Spice device simulator tool. It includes two stages, first stage includes 7 comparators and second stage has a thermometer encoder. The simulation is done in NG spice tool developed by university of California at Berkeley (USA).The response time of the comparator and ADC are 3.7ns and 4.9ns respectively with 50.01µw power dissipation which makes the ADC more suitable for high speed application with lower power devices.

*Keywords*— Flash ADC, Comparator, Thermocouple code, encoder, NGspice tool

## I. INTRODUCTION

Both data about the physical world and control signals sent to interact with the physical world are typically "analog" or continuously varying quantities. In order to use the power of digital electronics, one must convert from analog to digital form on the experimental measurement end and convert from digital to analog form on the control or output end of a laboratory system. Applications such as wireless communications and digital audio and video have created need for cost-effective data converters that will achieve higher speed.Fig.1 shows the basic block diagram for A/D conversion process as an interface between real time system and control system.

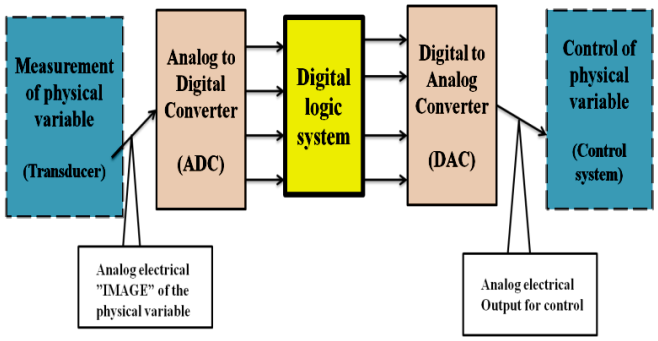


Fig.1 Block diagram for need of A/D process in real world

There are many types of ADC are reported such as flash ADCs, Pipelined ADCs, Successive approximation ADCs, Ramp ADCs and Delta sigma based ADCs each with unit architectures and different set of limitation.Fig.2 shows the general block diagram of general A/D conversion process for ADCs[1]. Among all the ADCs, Flash ADCs are the fastest with constraint of large area and high power consumption and suitable for moderate resolution (6 to 10 digits).

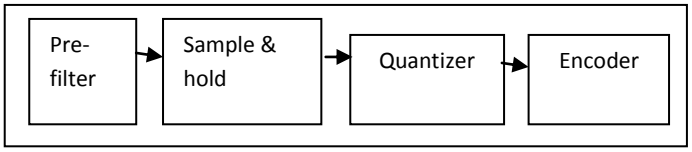


Fig.2 General Block diagram of ADC process

## II. ARCHITECTURE

Fig.3. shows a typical flash ADC block diagram. For an "N" bit converter, the circuit employs $2^{N-1}$ comparators. A resistive divider with $2^{N}$ resistors provides the reference voltage. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator in output is "0".

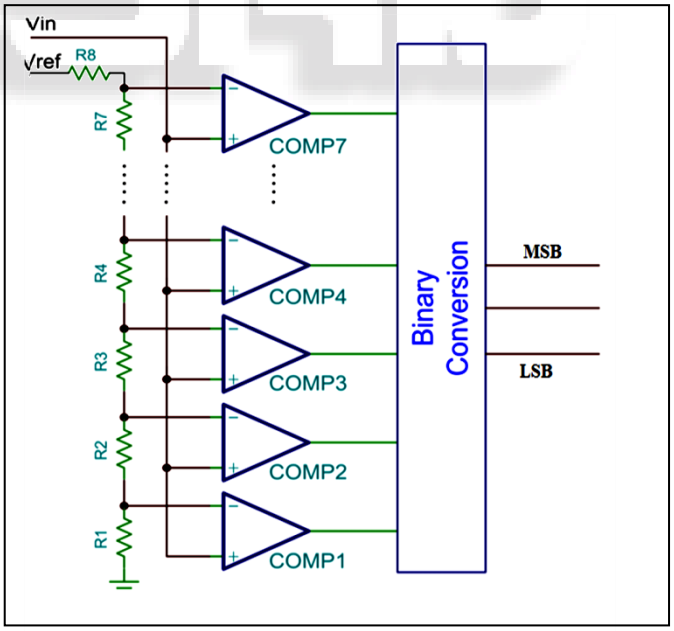


Fig.3 block diagram for 3bit FLASH ADC

As shown in Fig. 3, the flash ADC is composed of three major components: resistors string, comparators and encoder. The analog input voltage is compared to the reference voltage levels generated from resistors string and the speed of A/D conversion is therefore maximized [2]. The outputs of comparators form a thermometer code (TC) which is a combination of a series of zeros and a series of

 

ones, e.g., 000…011…111. Because binary code is usually needed for digital signal processing, a thermometer code is then transformed to a binary code through a (2k-1)-to-k TC-to-BC encoder, where k is the resolution (bits) of ADCs. The cost of such a traditional encoder increases exponentially with the resolution. Optimizations on area cost, circuit latencies and power consumptions are greatly expected. In this paper the higher conversion speed is achieved by reducing the delay time for each device by changing the W/L ratio of MOSFETs.

### A. Comparator Circuit

Figure 4 shows the circuit diagram for the comparator circuit used in proposed Flash ADC. Circuit the comparator consists of mainly three blocks connected in series

(1) Preamplifier:

The preamplifier stage improves sensitivity of a comparator by amplifying the differential signal across M1-M2, and isolates the input from the switching noise coming from positive feedback stage. In above fig. it is consisting of transistors M1 to M7.

(2) Regenerative or decision making circuit:

The positive feedback stage determines which of the input signal is a larger and it latches onto that. In this stage output is not rail to rail. It is having transistors M8 to M13.

(3) Output amplifier:

The output buffer amplifies output of positive feedback circuit and outputs digital signal. The transistors M14 to M19 are part of amplifier stage.

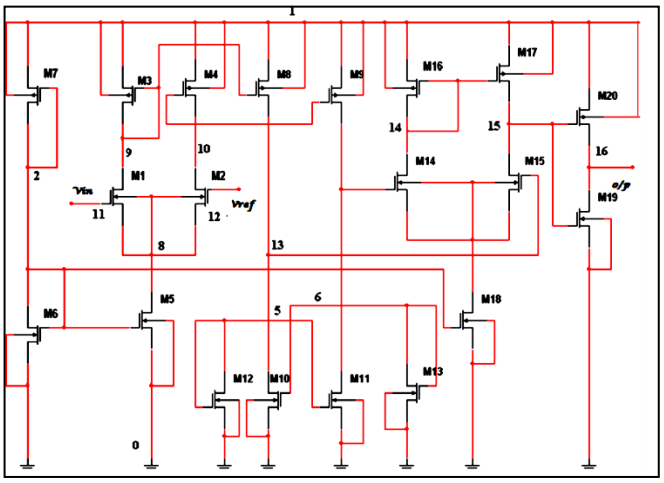


Fig.4 Circuit diagram for comparator

### B. Design of Thermometer to Binary Encoder

Unary coding, sometimes called thermometer code, is an entropy encoding that represents a natural number, n, with n ones followed by a zero (if natural number is understood as non-negative integer) or with n − 1 ones followed by a zero (if natural number is understood as strictly positive integer). For example 5 is represented as 111110 or 11110. Some representations use n or n − 1 zeros followed by a one. The ones and zeros are interchangeable without loss of generality. Unary coding is an optimally efficient encoding for the following discrete probability distribution [4]

$P(n) = 2^{-n}$ For n=1,2,3…… (1)

In symbol-by-symbol coding, it is optimal for any geometric distribution

$P(n) = (K-1)\,K^{-n}$ for which $k \geq \varphi = 1.61803398879\ldots$ (2),

Below table 1 shows the truth table for the 7 bit to 3 bit thermometer to binary encoder. The binary code can be obtained by using the K'MAP method and the total circuit is designed by the universal NAND gates. Figure 5 shows the basic gate level implementation for the encoder circuit. The gate delay for the inverter, 2-input,3-input and 4-input NAND gates are 0.29ns,0.51ns,0.37ns,1.06ns respectively with 2 ns rise time and fall time for inputs. The Boolean equations for outputs are given below.

o1 (MSB): D (3)

o2: E+C'E+E'F (4)

o3 (LSB): AB+B'C+D'E+F'G (5)

Table:1 Truth table for thermometer to binary encoder

| **Thermometer Code** | | | | | | | **Binary Code** | | |
|---|---|---|---|---|---|---|---|---|---|
| **A** | **B** | **C** | **D** | **E** | **F** | **G** | **o1** | **o2** | **o3** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Fig.6 shows the basic circuit for the inverter, 2-input NAND gate, 3-input NAND gate, 4-input NAND gates using MOSFETs. The response time for the gates can be optimized by the tuning the W/L ratio of NMOS and PMOS for each circuit. For the high speed ADC the response time for the gates, comparator, and encoder should will as small as possible.

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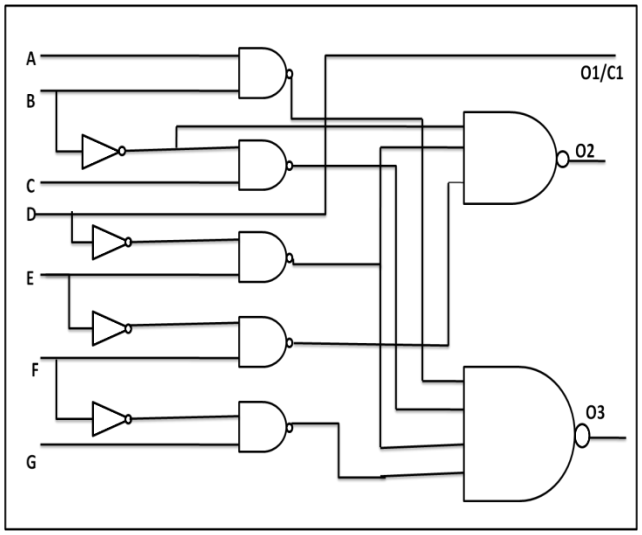


Fig.5 Gate level implementation of encoder

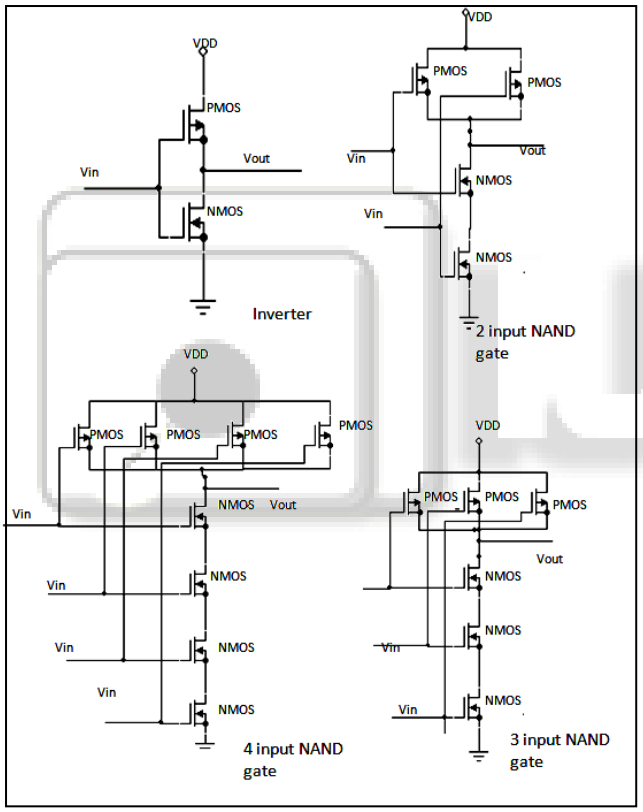


Fig.6 Circuits for the gates used in encoder

## III. SIMULATION ANALYSIS

Simulation for all the components of ADC such as NAND gates, encoders, comparators, inverters are done in the NG SPICE device simulator tool in 0.18µm technology. waveforms for all the outputs for respective component are shown in below figures.

### A. Comparator Output waveform

Figure 7 shows the graphical representation of input/output and reference voltage for the comparator. In figure 8 the response time for the comparator is plotted. We have achieved response time equal to 3.7ns.

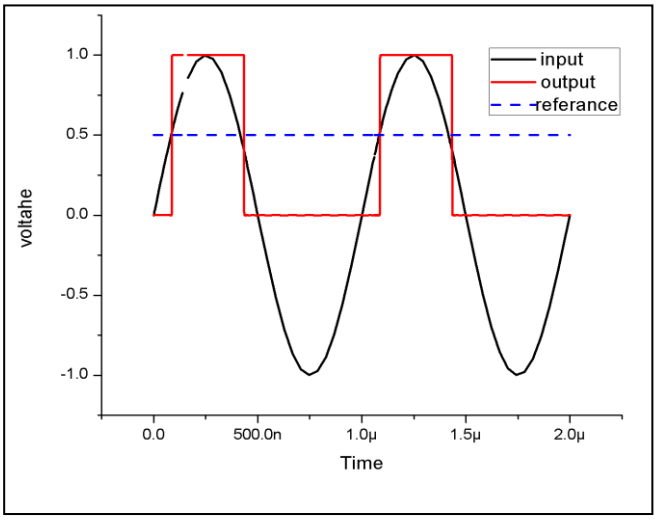


Fig.7 Simulation result for comparator output.

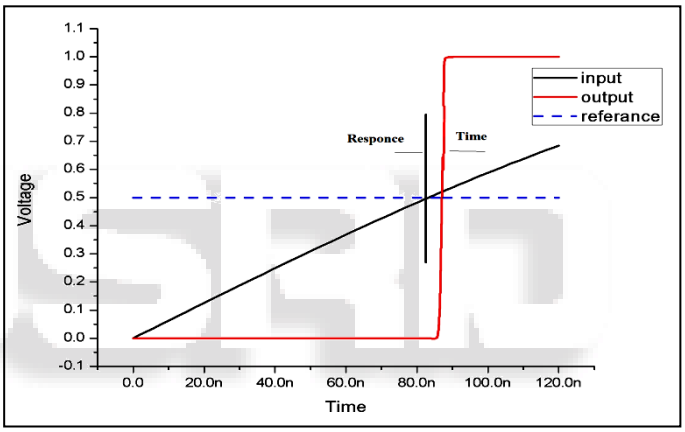


Fig.8 Simulation result for comparator response time.

### B. Output Waveforms for the gates used in encoder.

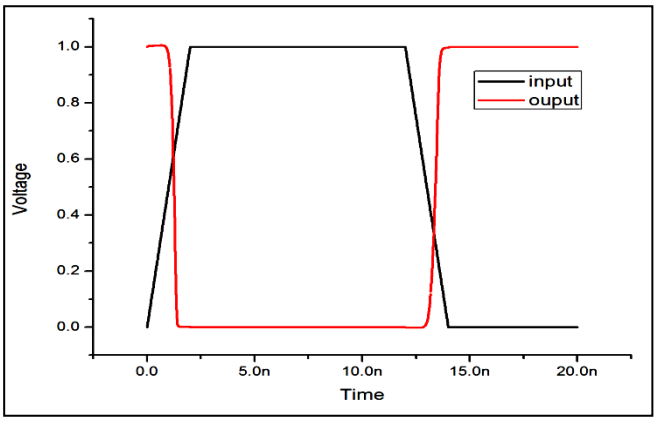


Fig.9 Simulation result for inverter circuit

Figure 9,10,11,12 shows the simulation result for the inverter,2-input NAND gate,3-input NAND gate and 4-input

NAND gate result respectively. Each simulation in carried out with the NG Spice tool with 180nm technology. The response time for the inverter,2-input NAND gate,3-input NAND gate and 4-input NAND gate are 0.24ns,0.17ns,0.39ns and 0.7ns respectively

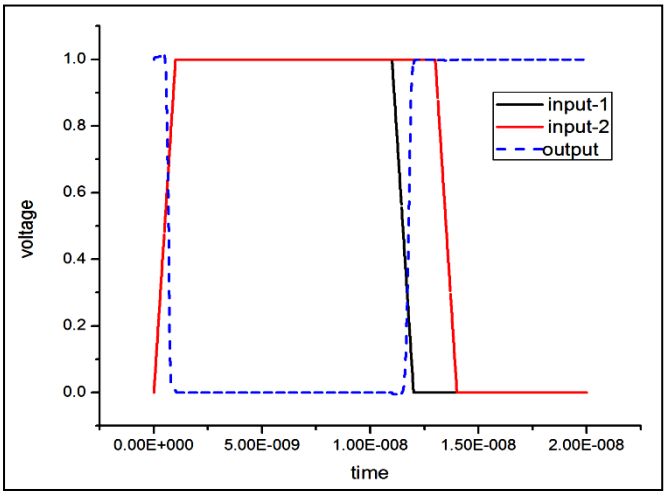


Fig.10 Simulation result of 2-i/p NAND gate.

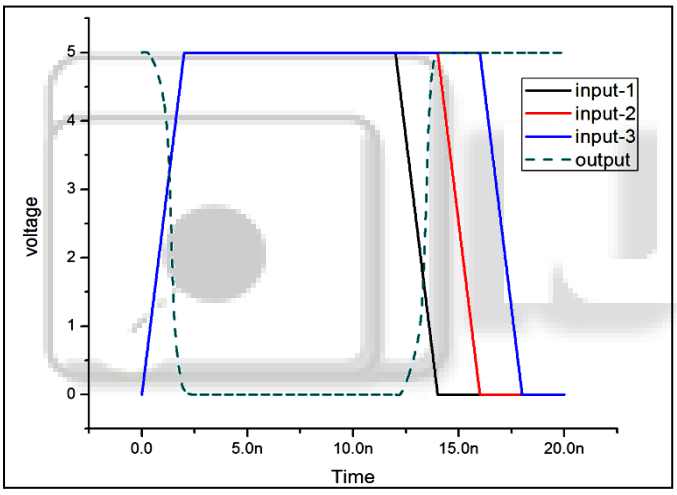


Fig.11 Simulation result of 3-i/p NAND gate..

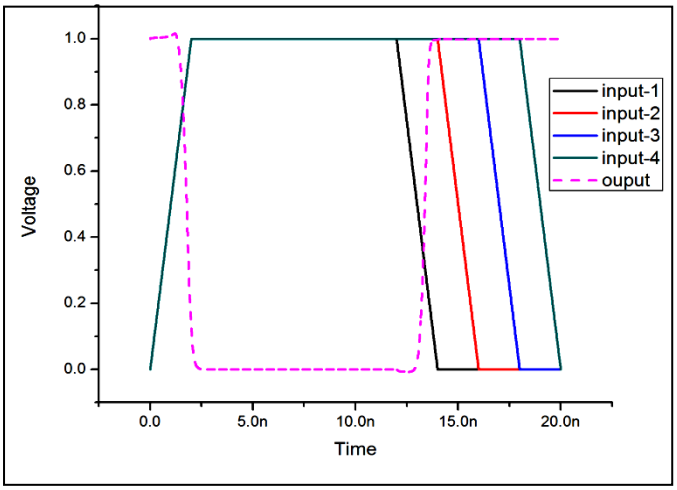


Fig.12 Simulation result of 4-i/p NAND gate.

C. 3 bit flash ADC output

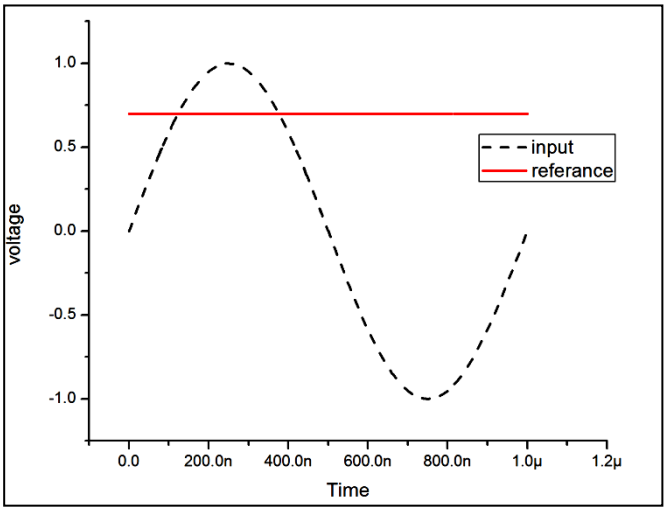


Fig.13 Simulation result for inputs of 3 bit flash ADC

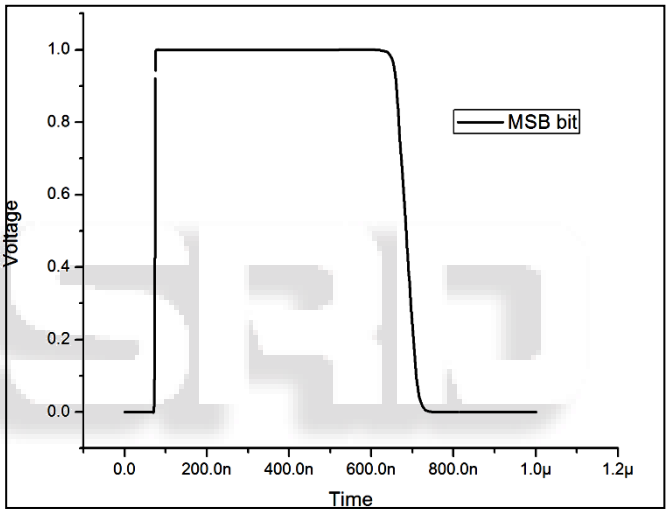


Fig.13 Simulation result for MSB bit of 3 bit flash ADC

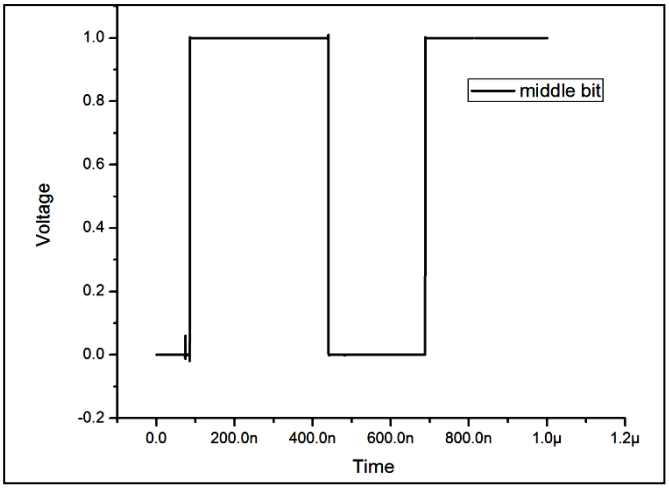


Fig.15 Simulation result for MIDDLE bit of 3 bit flash ADC

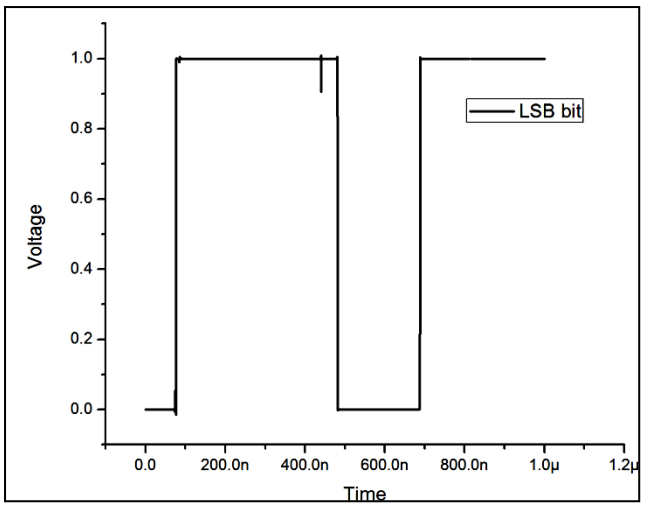


Fig.15 Simulation result for LSB bit of 3 bit flash ADC

## IV. CONCLUSION AND FUTURE WORKS

This paper provides the basic result of the 3 bit FLASHADC. Although this technique is very much costly due to the increase in complexity for higher resolution, it can be helpful in implementation of moderate resolution ADC. The most of power consumption of the ADC occurs in the comparator as expected. When the ADC is implemented for higher resolution then the power consumption is significant. It is very difficult to reduce the power consumption is FLASH ADC because the comparator are operating in parallel and so for the higher resolution and speed we have tradeoff with the power consumption.
Table 2 shows the performance parameter for the FLASH ADC.

Table: 2 Specification summary for the Flash ADC

| | |
|---|---|
| Technology | 0.18µm |
| Resolution | 3 Bit |
| Supply voltage | 1.0 v |
| Input voltage | 0 to 1 v |
| Comparator sensitivity | 11 mv |
| LSB | 0.125 v |
| Comparator response time | 3.7 ns |
| Unity Gain Bandwidth | 204.17 MHz |
| Comparator Gain | 28.86 DB |
| Phase Margin for Comparator | 49.3º |
| Slew rate | 6.28 v/µs |
| offset voltage of OP-AMP | 11.72 µv |
| power dissipation | 50.01 µW |
| ICMR | 0.25 to 0.75 v |
| Switching Voltage of comparator | 5 ms |

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