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Comparative Assessment of Multigate MOSFET Structures

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Abstract — Multigate MOSFETs (multiple-gate field-effect transistors) have recently emerged as promising alternatives to conventional planar MOSFETs, which are increasingly constrained by scaling limitations. As device dimensions continue to shrink into the nanoscale regime, planar transistors experience several challenges such as pronounced short-channel effects (SCEs), increased leakage current, and reduced electrostatic control over the channel. Multigate transistor structures address these issues by employing multiple gate electrodes that surround the channel region, thereby improving gate control over charge carriers and enhancing overall device performance. This work presents a comparative assessment of various multigate MOSFET architectures, including double-gate (DG), FinFET, tri-gate, Pi-gate, omega-gate, and gate-all-around (GAA) structures. The structural characteristics, operating mechanisms, and performance benefits of each architecture are examined with respect to their suitability for nanoscale device applications. Compared with planar MOSFETs, multigate transistors offer improved electrostatic control, higher drive current capability, effective suppression of short-channel effects and significantly reduced leakage current. In addition, the role of substrate engineering in multigate transistor fabrication is discussed, particularly the use of silicon-on-insulator (SOI) technology, which contributes to improved device isolation and performance. Among these architectures, FinFET and GAA transistors are considered highly scalable and suitable for future technology nodes. Consequently, multigate transistor structures are expected to play a vital role in extending Moore's Law and enabling the development of high-performance and energy-efficient integrated circuits.

Keywords: Multigate MOSFET, FinFET, Gate-All-Around FET, Nanowire Transistor, Silicon-on-Insulator

I. INTRODUCTION

For the past few decades, planar CMOS technology has completely transformed the electronics sector. Moore's law forecasted that shrinking of device size would occur quickly and predictably, and thus enabled the semiconductor manufacturing sector to create new products with expanded functionality for every new technological generation. The ongoing scaling of channel length, gate dielectric layer thickness, and power supply voltage reduction has yielded continuous improvements in transistor performance. These enhancements include fast operation, great scalability through small transistors, low power dissipation and cost savings per unit of functionality which drives to the most efficient electronic systems (1).

However, the scaling of transistors has faced major issues such as the emergence of SCEs. The decrease in device dimensions brings the source and drain regions closer together. The gate's potential to efficiently control the channel is limited by its close proximity. Accordingly, the presence of SCEs in scaled devices is enfolding their performance and causing a major obstacle to their continued downsizing (2).

In order to preserve the rate of enhancement in device performance with continued down scaling, advancement in device designs and fabrications are required. It has been proposed that a number of device topologies, such as fully depleted Silicon on Insulator (FD SOI) FETs and multigate FETs, can provide better electrostatic control of the channel and reduce SCEs. The Multigate MOSFET, with its progressive scalability, superior channel control through multiple gates, ideal subthreshold slope (SS), reduced leakage current and enhanced on/off switching characteristics, is optimal when compared to bulk MOSFETs for nanoscale integrated circuits. In comparison to conventional single gate MOSFETs, this structure's double-gate (DG), tri-gate, omega-gate, pi-gate, segmented-gate, gate-all-around (GAA), 3D stacked nanowire (NW), and nanosheet (NSH) MOSFETs perform better (3). Realizing volume inversion, especially in transistor architectures with high gate wrapping and channel regions perpendicular to carrier transport directions, could result in excellent gate control and mobility enhancement. However, while these factors benefit the control of SCEs and enhance the on-current (I_{ON}) in ultra scaled MOSFETs, they also result in a significant self-heating effect (SHE).

II. METHODOLOGY

Hyung Kyu-Lim et al.'s research (4) established that the bottom gate's main purpose in DG MOSFETs on an SOI substrate is to adjust or modify the top gate's threshold voltage (V_T). By encasing a FD SOI device among two gate electrodes coupled together, or what is known as an XMOS, T. Sekigawa et al. (5) proposed the self-aligned DG MOSFET to gain a considerable reduction of SCEs.

The concept of the first self-aligned vertical multigate MOSFET dubbed DELTA (Fully Depleted Lean Channel Transistor), was developed by D. Hisamoto et al. (6-7)

This transistor was built utilizing a "finger," "leg," or "fin" shaped silicon island, which is tall as well as thin. With the exception of a dielectric layer known as "hard mask" placed over the silicon fin, the FinFET construction resembles the DELTA construction. The hard mask is utilized to stop parasitic inversion channels forming at the device's upper corners.

In addition to double-gate SOI MOSFETs, there have been advancements in multigate transistor designs like triple-gate and GAA devices. A triple-gate FET consists of a thin silicon fin with gate electrodes on three sides (8), whereas a GAA FET is a planar transistor in which the channel is completely surrounded by the gate electrode (9).

Several new variants of vertical-channel, DG SOI MOSFETs have been introduced, including the Silicon-on-Nothing, Multi-Fin XMOS, triangular-wire SOI, and Δ -

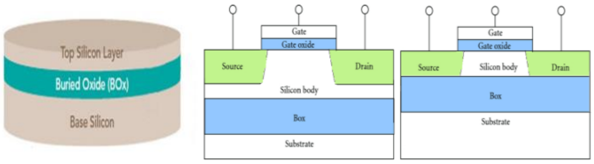
channel SOI MOSFETs (10). The tri-control gate surrounding gate transistor (TCG-SGT) was recommended by Takuya Ohba et al. (11) to achieve improved gate control over the channel. Examples of surrounding gate MOSFETs are the pillar surrounding-gate MOSFET (cross section square), the planar surrounding-gate devices (cross section square or circular), and the CYNTHIA device (cross section circular).

A. Silicon on Insulator

Substrate engineering has revolutionized the IC industry by overcoming traditional scaling limitations. It has led to a strong coupling between device architecture and engineered substrates, a coupling that strengthens as the semiconductor manufacturing sector advances to the 32 nm process nodes and beyond. With the deployment of SOI wafers in the late 1990s, substrate engineering gathered speed. Improved current drive capability, diminished leakage currents, and lower parasitic capacitance were made possible by SOI substrates, which enhanced IC functionality and reduced power (12). SOI substrates are widely utilized in various applications, including image sensors, MEMS, high voltage and smart power circuits, silicon-based optoelectronic devices, RF circuits, and other cutting-edge technologies.

One of the main differences between ordinary MOS devices and SOI devices is that the latter have a buried oxide (BOX) layer that electrically isolates the body from the substrate. Three layers make up SOI wafers: a top silicon layer (where transistors are made), an insulating material beneath it, and base silicon, as seen in Fig. 1(A). On the basis of the thickness of the Si body, SOI devices are classified as partially and fully depleted (PD and FD) SOIs.

The Si body of PDSOI MOSFETs is thick, and the deepness of the depletion area beneath the gate is less than the body thickness, allowing them to behave similarly to bulk MOSFETs to some extent. However, they suffer from a drawback known as the floating body effect. This implies that the body voltage is influenced by the device's previous condition, which can alter the threshold voltage and give rise to a parasitic bipolar transistor. FDSOI devices have a thin Si body that enables the depletion region to cover the entire body, effectively eliminating the floating body effect. Better electrostatic coupling among the top and bottom gates is made possible as a result. For sub-100nm CMOS applications, FDSOI MOSFETs are therefore the most appealing because to their acute SS and shorter body effect (13). The PDSOI and FDSOI MOSFETs cross sections are shown in Fig.1 (B) and Fig.1 (C).



(A) (B) (C)

Fig. 1: (A) SOI wafer, (B) PDSOI and (C) FDSOI MOSFET structures

Because of variables (14) like BOX, back gate bias, body thickness, and substrate doping, SOI MOSFETs offer versatility in terms of architecture. Scalability, SS, current drive, and transconductance all make them very appealing.

B. Multigate Transistors

A multigate or multiple gate transistors, is a type of MOS device that contain multiple gates instead of the single gate found in bulk MOSFETs. Rather than the number of separate gates, the term "multigate" refers to gate electrodes positioned on multiple sides of the Si body (15). These transistor architectures provide a larger drive current, enhanced resistance to SCEs, and improved gate control of the channel since they have a higher number of effective gates. The different kinds of multi-gate devices are as follows: single, double, triple, and quadruple gates.

C. Double-Gate MOSFET

One of the alluring topologies for sub-50 nm device creation is the DG FET. The main idea behind a DGFET is to utilize an extremely narrow Si channel and regulate it by applying gate contacts (front and back) on two flanks of the channel (16). The double gate topology is derived from thin film MOSFET structures such as FD-SOI, where the ground plane can function as the second (back or bottom) gate when BOX thickness is reduced to be comparable to that of the gate dielectrics. But in such a ground-plane configuration, the capacitance would be excessively high between the drain and the bottom conductor which results in poor switching performance. To improve the switching performance a second gate is positioned beneath the silicon layer. This gate containing a minimal overlap with the source and drain areas and can act as the bottom conductor. This configuration forms a DG MOSFET (17), as illustrated in Fig. 2. In this structure, there is no region separating the gate electrodes from the conducting channel, enabling more effective channel control through the simultaneous action of the two gates on the thin silicon body. The thin SOI layer creates a strong and permanent electrostatic coupling between the front and back gates. This coupling influences the overall electrical characteristics of the device.

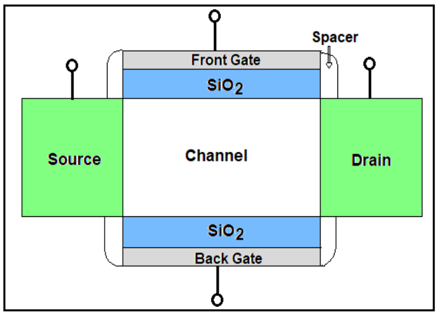


Fig. 2: Double Gate MOSFET structure

Depending on the gate biasing conditions, the DG MOSFET can be classified into three configurations: Symmetric Double Gate (SDG), Asymmetric Double Gate (ADG), and Ground Plane (GP) MOSFETs. In an SDG MOSFET configuration, both gate electrodes have identical work functions and are driven by the same input voltage, resulting in a symmetric electric field distribution within the channel region. In contrast, an ADG MOSFET configuration occurs when asymmetry exists between the two gates. This may arise either from different voltages applied to the two gates or from differences in their work functions, even when the same input voltage is applied. Such conditions produce an imbalance that leads to a non-uniform electric field distribution across the channel. In a GP MOSFET configuration, one gate electrode receives the input signal while the other gate is maintained at a constant bias voltage. Consequently, the electric field distribution within the channel becomes asymmetric, which influences the overall electrical characteristics of the device (18).

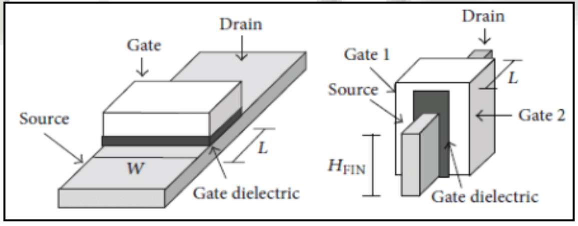
DGFETs offer the following benefits because of the enhanced electrostatic control provided by the two gates over the channel: The channel doping levels of DGFETs can be very low or even totally undoped, which allows for an accelerated switching speed. Additionally, the current driving ability of DGFETs is double that of planar CMOS. SCEs are readily suppressed. High carrier mobility within reduced dimensions.

D. FINFET

The declining performance of Planar MOSFETs in short-channel regimes has led to increased interest in FinFET technology in recent years. A FinFET is a non-planar transistor in which the channel formed in a thin vertical fin-shaped body. The thin silicon fin of the FinFET is mounted on a substrate. The channel can be precisely regulated because the gate surrounds it on three sides. The name of this structure comes from its Si body, which resembles the rear fin of a fish.

In FinFETs, channel is formed vertically along the height of the fin structure, unlike in planar MOSFETs where the channel is horizontal (19). In this structure, the effective channel width is determined by the fin height (H_{fin}), while the channel length (gate length) represents the physical distance between the source and drain regions along the channel direction.

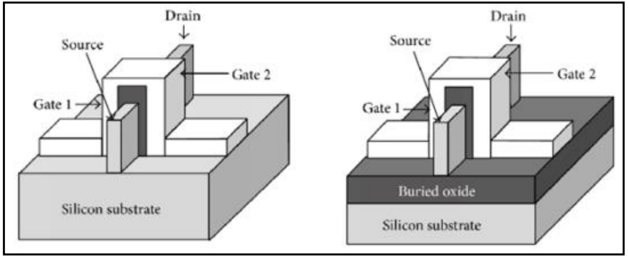
The structural difference between planner MOSFET and FinFET is depicted in Fig. 3.



(A) (B)

Fig. 3: Structural view of (A) Planner MOSFET (B) FinFET (19)

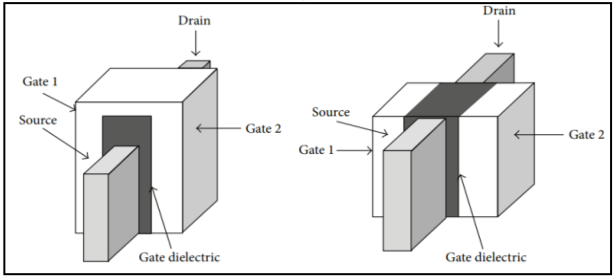
FinFETs can be manufactured on bulk silicon or on SOI wafers in terms of wafer technology. Fins in bulk FinFETs are all connected by a common silicon substrate while fins in SOI FinFETs are physically detached as illustrated in Fig. 4.



(A) (B)

Fig. 4: Architectural view (A) Bulk FinFET and (B) SOI FinFET structures (19)

Many organisations choose the bulk technology because the transition from conventional bulk MOSFETs to bulk FinFETs is relatively simple. In addition, FinFETs fabricated on both bulk and Silicon-On-Insulator (SOI) substrates exhibit comparable performance characteristics in terms of cost, yield, and device performance. FinFET structures can be implemented in several configurations depending on the number of terminals. Typically, FinFETs are classified into two main categories: independent-gate (IG) FinFETs, also known as four-terminal (4T) FinFETs, and shorted-gate (SG) FinFETs, also referred to as three-terminal (3T) FinFETs, as shown in Fig. 5.

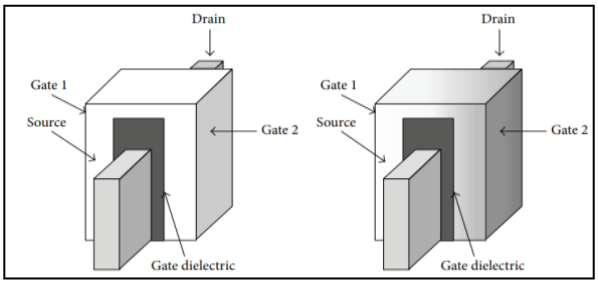


(A) (B)

Fig. 5: Device structures of (A) SG FinFET (B) IG FinFET (19)

In contrast to IG FinFETs, which have physically separated front and rear gates, SG FinFETs have both gates shorted, based on structural details. Both gates work together in SG FinFETs to regulate the channel's electrostatics. As a result, compared to IG FinFETs, SG FinFETs generally provide higher drive current (I_{on}) but they also tend to exhibit increased leakage current (I_{off}). Conversely, IG FinFETs employ electrically isolated gates, allowing independent biasing of the front and back gates. This feature enables linear control of the front-gate threshold voltage through the application of back-gate bias. The major difficulty offered by the IG Fin FET is that increase in chip area.

In conventional FinFET device, the front and rare gates typically possess identical work functions. However, when the work function of one gate differs from that of the other, an asymmetry is created between the two gates that control the channel. This structure is referred to as an Asymmetric SG-FinFET (ASG-FinFET) as shown in Fig. 6. FinFET devices designed with the ASG-FinFET configuration exhibit improved short-channel characteristics compared to SG-FinFET devices. In addition, they show a significant reduction in the off-state current (I_{off}). However, the on-state current (I_{on}) is generally slightly lower than that of SG-FinFET devices.



(A) (B)

Fig. 6: Schematic view of (A) SG FinFET and (B) ASG FinFET (19); shaded gate area indicates modified work function.

FinFET devices can be further classified into Double-Gate (DG) and Triple-Gate structures depending on the gate configuration and dielectric thickness (20). The primary difference between these two architectures lies in their gate structures. In a DG-FinFET, the top surface of the fin is covered with a hard mask, which prevents the formation of a gate in that region. Consequently, only the two side gates participate in controlling the channel, as illustrated in Fig. 7(A). The effective channel width of a DG-FinFET can be expressed as follows:

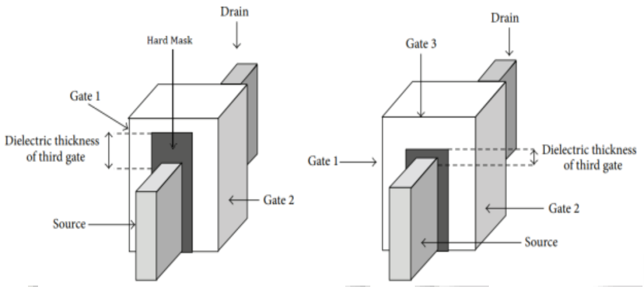
$$W_{eff} = 2nH_{fin}$$

Where n is the total number of fins and H_{fin} is the fin height.

As the dielectric layer on top of the silicon fin becomes thinner, as shown in Fig. 7(B), the third gate will be generated in a tri-gate device. Therefore, the third gate's presence causes the device's Weff to grow. The Tri-gate Weff is therefore:

$$W_{eff} = 2nH_{fin} + W_{fin}$$

where W_{fin} denotes the fin's width.



(A) (B)

Fig. 7: Architectural view of (A) DG FinFET and (B) Triple gate FET (19).

E. *Tri Gate FET*

Manufacturing FinFET structures using bulk-Si wafers require narrow Si fins with uniform width and a high aspect ratio (fin height to fin width). In addition, a deep retrograde doping profile at the fin base is necessary to suppress sub-fin leakage among source and drain areas (21).Contrarily, tri-gate structures allow for less retrograde channel doping and do not require thin, high aspect ratio Si fins to prevent DIBL.

In Triple-Gate MOSFET architecture, a single gate electrode surrounds three sides of the fin, forming a square or rectangular cross-sectional structure. Since the gate controls the channel from three sides, the electric field above the fin is not screened, resulting in stronger electrostatic control over the channel. This configuration effectively increases the available conduction area for charge carriers, thereby improving device performance (17).

To maintain full substrate depletion in single-gate transistors, the silicon body thickness (T_{si}) needs to be approximately one-third of the gate length (L_g). Tsi is equal to 2/3 of Lg in double-gate systems since each gate regulates half the Tsi. The tri-gate transistor has a larger W_{fin} and a lower H_{fin} relative to a double-gate transistor. A part of the silicon surface is under the control of each gate in the tri-gate device. The silicon body must be completely depleted to achieve full depletion, and this can be accomplished by concurrently changing the silicon fin's height and width. (22). Device dimensions for a tri-gate FET should be

L_g = silicon body width = silicon body height.

Because of this, the tri-gate MOSFET can achieve higher electrostatic integrity (and hence, scalability) than the double-gate FinFET without requiring the fabrication of subgate-length. So finally, the Tri-gate MOSFET allows a better gate electrostatic control of conducting channel, less leakage, Lower power consumption, less sensitivity to change in V_T with respect to channel length and Enhanced scalability. The major drawback offered by this device is

Corner effect which indicates trapped charges appear at the corner edges. It leads to high temperatures, reliability problems and worsened SCEs. Rounding of corners is the most efficient solution to address the corner effect (17).

By spreading the gate electrode's sidewalls into BOX beneath the channel region and down to a specific depth, it is possible to further improve the gate control over the Tri-gate FET's channel electrostatics. The reason these devices are referred to as "Pi FinFET" and "Omega FinFET" is that their gates are wrapped around semiconductor bodies in a manner that resembles the Greek letters Pi (Π) and Omega (Ω). These devices range in effective gate count from three to four.

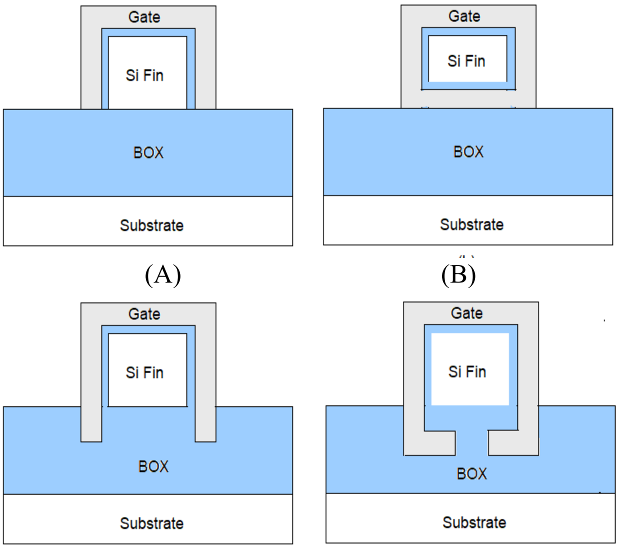
F. *Pi FET*

Both double-gate SOI MOSFETs (front and rear gate) and normal GAA devices can lower SCEs; however, the fabrication procedure required for these devices cannot be readily integrated with SOI CMOS or conventional CMOS technology. Fig. 8(C) shows the simple Pi-FET gate construction that starts with a triple-gate MOSFET. The gate electrode protrudes into the BOX to a specific depth on both sides of the device (23). With this preparation, there are now 3.12 gates instead of just 3. The extension of the gate into the BOX effectively protects the rear side of the channel region from the electric field originating from the drain, almost equivalent to the action of a true back gate. To create the Pi FET, in addition to the SOI CMOS fabrication procedure, it further needs masking and a RIE BOX etch phase (24).

With a High-K dielectric, metal gate, and HfO2 (Hafnium dioxide) as the best dielectric material for forthcoming nanoscale multi-gate SOI devices, Fatima Zohra Rahou et al.(25) carry out 3D simulation of Pi gate SOI FETs.

G. *Omega FET*

The gate structure of the Omega FET, as illustrated in Fig. 8(D) is comparable to that of the GAA FET and is produced using a manufacturing process similar to those used for FinFETs. Resembling a traditional Ultra-Thin-Body SOI transistor, the Ω -FET has a top gate, sidewall gates akin to FinFETs, and gate expansion underneath the channel. The gate almost wraps around the transistor's body, like the GAA structure. In actuality, the GAA transistor-like structure is increasingly apparent the longer the gate extension. Apart from mitigating DIBL by concealing electric field lines from the drain, Ω-FETs' gate extension additionally improves gate-to-channel controllability. (26).



(A) (B)

(C) (D)

Fig. 8: Cross sectional view of (A) Triple- gate (B) GAA (C) π- gate (D) Ω - gate MOSFETs

Perina et al. (27) evaluated the analog performance of n- and p-type nanowire Omega (Ω)-gate MOSFETs using key parameters such as intrinsic gain (A_V) and unit gain frequency (f_t). Their analysis also examined the impact of device dimensions on these parameters. Chen et al. (28) reported Ge n-channel Ω-gate MOSFETs integrated on a Si platform with a [010] oriented channel and a high-k dielectric/metal gate stack. They found that the Ω-gate structure effectively SCEs. Barraud et al. (29) developed cylindrical silicon nanowire (NW) MOSFETs incorporating a Ω- shaped gate, achieving strong electrostatic control even for nanowire diameters as small as 8 nm. In addition, they showed that variations in SiN spacer thickness significantly influence the short-channel performance of Ω-gate nanowire MOSFETs (ΩGNW), making them a suitable compromise among MuGFET devices for maximizing electrostatic confinement while minimizing fabrication complexity.

H. GAA FET

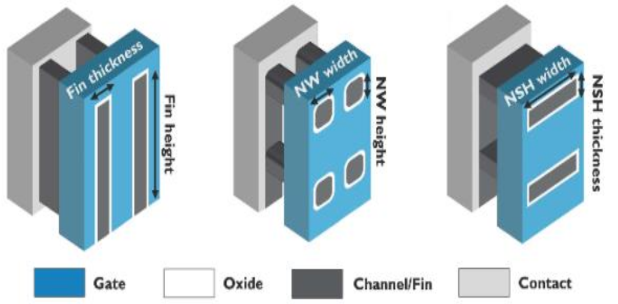
At the 22 nm technology node, Intel introduced the FinFET architecture, which rapidly became the dominant transistor technology for advanced semiconductor manufacturing. Due to the continues improvements in scaling the FinFET structure encountered various challenges like poor control over the off-state currents and faced several SCEs. To overcome these challenges, an architectural change emerged in the form of GAA structure (30).

In GAAFET, the gate electrode, typically made of poly silicon, is formed above an active silicon channel that is separated by a thin gate oxide layer (31). The structure of a GAAFET, illustrated in Fig. 8(B) features a gate that encloses the channel from all sides, including the front, back, and the two lateral surfaces. Because the gate surrounds the channel completely, this configuration is referred to as a “gate-all-around” structure, creating four interfaces between the gate and the channel.

Two added gates create two extra inversion channels, allowing further downsizing of devices in contrast to DG MOSFETs (32).

Based on the orientation and structure of the channel, GAAFETs can be classified into different types. The former can be classified as lateral and vertical, while the latter can be further divided into nanowire (NW) and nanosheet (NSH) structures. Lateral GAAFETs have a horizontal channel orientation, while the vertical GAAFETs have a channel orientation perpendicular to the semiconductor substrate. Another type, known as Nanowire GAAFETs, utilizes a nanowire as the channel structure, which can be either cylindrical or rectangular in shape show in Fig. 9(B). The nanowire channel is fully wrapped by the gate material, providing control from all sides. In contrast, nanosheet GAAFETs as depicted in Fig. 9(C) employ a channel structure composed of multiple stacked nanosheets. These nanosheets are extremely thin, and the gate material surrounds them.

Two kinds of channel structures exits in Lateral GAAFETs and are called as LNWGAAs (Lateral Nanowire Gate-All-Around transistors) and LNSHGAAs (Lateral Nanosheet Gate-All-Around transistors) (33).



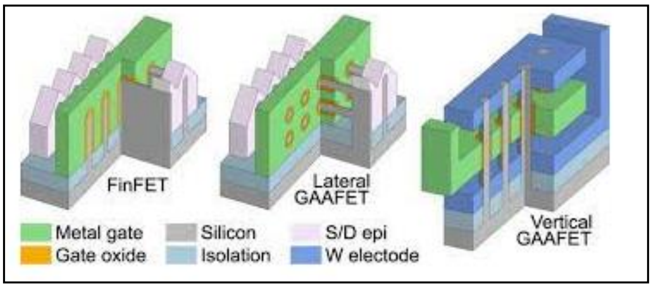
(A) (B) (C)

Fig. 9: Structural comparison of (A) FinFET, (B) Nanowire-GAAFET, and (C) Nanosheet-GAAFET (34)

In LNWGAAs, the channel's circumference or diameter controls the device's process node and W_{eff}. It is possible to extend the spacing between nanowires (NWs) in order to sustain current levels, although doing so could raise parasitic capacitance. Fabricating nanowire devices is challenging due to process differences including line edge roughness and nanowire size.

LNSHGAAs offers reduced parasitic capacitance and improves the current driving capability compared to LNWGAAs but the difficulty is that it occupies larger footprint. The difficulty facing in lateral GAAFETs is with the contacted gate pitch (CGP). To overcome this, vertical GAAFETs as illustrated in Fig. 10(C) are used. In this the channel is oriented vertically rather than horizontally. This feature gives the advantages, including relaxed gate length and spacer. Aside from that, because it utilizes 3D space, it can also lower the layout of the device.

Based on their channel topologies, vertical GAAFETs are further divided into CLGAAs (CyLindrical GAA transistors) and CLJLGAAs (CyLindrical Junction Less GAA transistors).



(A) (B) (C)

Fig. 10: 3D view of (A) FinFET, (B) LNWGAA and (C) CLGAA MOSFETs (35)

The cylindrical shape of the channel gives rise to the vertical NWGAAs, also known as CLGAAs. By loosening the CGP, more nanowires can fit into the same area as LNWGAAs, reducing the device footprint of CLGAAs. Because of its circular channel and body design, these devices can prevent corner effects and consume other benefits of this arrangement include perfect SS, CMOS capability, and the elimination of the floating body phenomenon.

Although CLJLGAAs and CLGAAs share the same structure, CLJLGAAs have the same channel, source, and drain doping concentration. Due to the continuous doping across three locations, the term "junctionless" was employed. Because CLJLGGA has the lowest leakage current and threshold voltage roll-off, it is better suited for low power electronics. Its Ion is, however, substantially less than that of the other three structures.

III. RESULTS AND DISCUSSION

Compared to standard planar MOSFET structures, multigate MOSFETs will experience significantly improved performance. Both double-gate (DG) and FinFET devices have better electrostatic control of the channel than single-gate planar devices, which results in improved suppression of short-channel effects. Both tri-gate and Pi-gate devices further enhance the gate control capability over the channel by increasing the effective gate coverage area above and below the channel region.

Among all of the multigate devices discussed, the gate-all-around (GAA) MOSFET has the best electrostatic integrity due to the fact that the gate surrounds the channel completely. This configuration will significantly reduce leakage current and also improve the I_{ON}/I_{OFF} ratio.

In addition, both Omega-gate (Ω-G) and nanowire-based GAA devices also demonstrate excellent scalability for future technology nodes; however, with each successive level of gate architecture advancement, fabrication complexity will continue to increase. For this reason, FinFET technology has been widely adopted in modern semiconductor manufacturing, while gate-all-around (GAA) transistors are expected to become the primary device architecture for sub-5 nm technology nodes.

Device Structure	**Gate Control**	**Leakage Current**	**Fabrication Complexity**	**Scalability**
SOI MOSFET	Moderate	Moderate	Low	Limited
Double-Gate MOSFET	High	Low	Medium	Good
FinFET	Very High	Low	Medium	Very Good
Tri-Gate FET	Very High	Low	Medium	Very Good
Pi-Gate FET	Very High	Very Low	High	Excellent
Omega-Gate FET	Very High	Very Low	High	Excellent
Gate-All-Around (GAA) FET	Excellent	Extremely Low	Very High	Outstanding

Table 1: Comparison of Multigate MOSFET Structures

IV. CONCLUSION

The continued development of Deep Submicron based designs and architectures, along with the increasing need for fast and ultra-energy efficient integrated circuits, has made the planar MOSFET transistor a barrier. One major shortcoming of planar transistors is the occurrence of SCEs when the channel length is reduced. Planar MOSFET inadequacies can now be minimized with the help of multi-gate FETs. These devices come in a range of forms and sizes and allow chip makers to construct transistors with shorter channel lengths, which lead to lower power consumption and higher switching rates. In order to increase their electrostatic integrity and lessen scaling effects such short channel effects, this research emphasizes the relevance of increasing the effective number of gates in MOSFET devices.

Different multigate configurations, including gate-all-around, Trigate, and double-gate, are covered in this work. Better performance and a high I_{ON}/I_{OFF} ratio are generated by the double-gate constructions, where gates are positioned on both sides of the channel. In contrast, the FinFET structure successfully suppresses variability brought on by random oscillations in the dopant by utilizing a thin channel region. The Trigate structure is particularly well suited for fully-depleted transistor applications because it provides three times as much space for electrons to traverse. This increases device efficiency. The gate-all-around arrangement, which completely surrounds the channel with gate material to improve transistor control and performance, also considerably improves carrier movement. All things considered, multi-gate FETs have revolutionized chip technology by eliminating previous limitations and providing opportunities for ever more efficient and implementable system on chip design.

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B. Conflict of Interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

C. Author Contributions

- Lakshmi Barla: Conceptualization, Literature review, Writing – Original Draft.
- Mamidipaka Hema: Supervision, Technical review, Validation.
- Kaparapu Babulu: Review and Editing, Guidance and manuscript improvement.

D. Ethics Approval

This study does not involve human participants or animals. Therefore, ethical approval was not required.

E. Data Availability

The data supporting the findings of this study are available within the article and its references.

F. Abbreviations

- MOSFET – Metal Oxide Semiconductor Field Effect Transistor
- SCE – Short Channel Effects
- SOI – Silicon on Insulator
- FinFET – Fin Field Effect Transistor
- GAAFET – Gate All Around Field Effect Transistor
- DG – Double Gate

REFERENCES

[1] P. Vimala and Rakshith N V, “Comparative Study of Multi-gate Nanowire Field Effect Transistor,” *J of Nanotechnology and Nano-Engineering*, 2019; vol.5(3): pp.1-9

[2] Neeraj G. “Performance Enhancement of Multigate MOSFET Using Engineering Technique-A Review,” *International Journal of Research and Analytical Reviews.* Apr.-Jun 2019; vol.6(2)

[3] Sun Y, Yu X, Zhang R, Chen B, and Cheng R, “The past and future of multi-gate field-effect transistors: Process challenges and reliability issues,” *J. Semicond.,* 2021, 42(2), 023102.

[4] Hyung-Kyu Lim and Jerry G Fossum, “Threshold Voltage of Thin-Film Silicon-on-Insulator (Sol) MOSFETs,” *IEEE Trans. Electron Devices*, vol. ed-30, no. 10, Oct. 1983,pp.1244-1251.

[5] T. Sekigawa and Y. Hayashi, “Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate,” *Solid-State Electronics*, vol. 27, nos 8/9, pp. 827-828, 1984.

[6] D. Hisamoto, T. Kaga, Y. Kawamoto, E. Takeda, “A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra-thin SOI MOSFET,” *Technical Digest of IEDM* (1989) 833.

[7] D. Hisamoto, Wen-Chin Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, Tsu-Jae King, J.Bokor and Chenming Hu, “FinFET-a self-aligned double-gate MOSFET scalable to 20 nm,”. *IEEE Trans. On Electron Devices*, vol. 47, no. 12, Dec. 20004,pp.2320-2025.

[8] M.C. Lemme a, T. Mollenhauer a , W. Henschel a , T. Wahlbrink a , M. Baus b , O. Winkler b , R. Granzner, F. Schwierz c , B. Spangenberg b and H. Kurz, “Subthreshold behavior of triple-gate MOSFETs on SOI material” Solid-State Electronics 48 (2004) 529–534.

[9] J.P. Colinge, M.H. Gao, A. Romano, H. Maes, and C. Claeys, “Silicon-on-insulator “gate-all-around device”,” *Technical Digest of IEDM* (1990) 595.

[10] J.P. Colinge, “Multi-gate SOI MOSFETs,” *Microelectronic Engineering* 84 (2007) 2071–2076.

[11] Takuya Ohba a, Hiroki Nakamura a , Hiroshi Sakuraba b ,and Fujio Masuoka, “A novel tri-control gate surrounding gate transistor (TCG-SGT) nonvolatile memory cell for flash memory” *Solid-State Electronics* 50 (2006) pp.924-928.

[12] Bich-Yen Nguyen, George Celler, and Carlos Mazure, “A Review of SOI Technology and its Applications*,” Journal Integrated Circuits and Systems* 2009; v.4 / n.2:51-54.

[13] Rituraj Singh, “Partially and Fully Depleted SOI MOSFETs,” Aug. 2014.

[14] Thomas Ernst, Sorin Cristoloveanu, Gérard Ghibaudo, Thierry Ouisse,Seiji Horiguchi, Yukinori Ono, Yasuo Takahashi and Katsumi Murase, “Ultimately Thin Double-Gate SOI MOSFETs ,” *IEEE Trans. Electron Devices*, Vol. 50, No. 3, Mar. 2003.

[15] A. Breed and K. P. Roenker, "Comparison of the scaling characteristics of nanoscale silicon N-channel multiple-gate MOSFETs," *48th Midwest Symposium on Circuits and Systems*, 2005., Covington, KY, USA, 2005, pp. 603-606 Vol. 1, doi: 10.1109/MWSCAS.2005.1594173.

[16] S. K. Gupta, G. G. Pathak, D. Das and C. Sharma, "Double Gate MOSFET and its application for efficient digital circuits," 2011 *3rd International Conference on Electronics Computer Technology*, Kanyakumari, India, 2011, pp. 33-36, doi: 10.1109/ICECTECH.2011.5941650.

[17] K. Garg, and Dhiraj Kapoor, “Single Gate Devices to Multigate Devices: A Review,” *International Journal of Innovations in Engineering and Management*, Vol. 4; No. 1: ISSN: 2319-3344 (Jan-June 2015).

[18] M. Z. Sadi, N. Karmakar, M. K. Alam and M. S. Islam, "Comparative analysis of subthreshold swing models for different double gate MOSFETs," *2008 International Conference on Electrical and Computer Engineering*, Dhaka, Bangladesh, 2008, pp. 152-157, doi:10.1109/ICECE.2008.4769191.

[19] Bhattacharya. D & Jha, N. K. (2014). FinFETs: From devices to architectures. Advances in Electronics, 2014, 1–21. https://doi.org/10.1155/2014/365689.

[20] Maurya, R. K., and Bhowmick, B. (2022). Review of FinFET devices and perspective on circuit design challenges. Silicon, 14(11), 5783–5791. https://doi.org/10.1007/s12633-021-01366-z.

[21] B. Ho, X. Sun, C. Shin and T. -J. K. Liu, "Design Optimization of Multigate Bulk MOSFETs," in *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 28-33, Jan. 2013, doi: 10.1109/TED.2012.2224870.

[22] Chau, R., Doyle, B., Kavalieros, J., Barlage, D., Murthy, A., Doczy, M., Arghavani, R., & Datta, S. (2002). Advanced depleted-substrate transistors: Single-gate, double-gate and Tri-gate. *Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials*.

[23] Jong-Tae Park, J. -P. Colinge and C. H. Diaz, "Pi-Gate SOI MOSFET," in *IEEE Electron Device Letters*, vol. 22, no. 8, pp. 405-406, Aug. 2001, doi: 10.1109/55.936358.

[24] Jong-Tae Park and J. -P. Colinge, "Multiple-gate SOI MOSFETs: device design guidelines," in *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2222-2229, Dec. 2002, doi: 10.1109/TED.2002.805634.

[25] Rahou, F. Z., Bouazza, A. G., & Bouazza, B. (2016). Performance improvement of pi-gate SOI MOSFET transistor using high-*k* dielectric with metal gate. *IETE Journal of Research*, *62*(3), 331–338. https://doi.org/10.1080/03772063.2015.1084898.

[26] Fu-Liang Yang *et al.*, "25 nm CMOS Omega FETs," *Digest. International Electron Devices Meeting,* San Francisco, CA, USA, 2002, pp. 255-258, doi: 10.1109/IEDM.2002.1175826.

[27] Perina, W. F., Martino, J. A., & Agopian, P. G. D. (2020). Analysis of omega-gate nanowire SOI MOSFET under analog Point of View. *JICS. Journal of Integrated Circuits and Systems*, *15*(1), 1–6. https://doi.org/10.29292/jics.v15i1.113.

[28] Chen, C. W., Chung, C. T., Tzeng, J. Y., Luo, G. L., & Chien, C. H. (2013). Ge N-channel omega-gate field effect transistors with [010] channel direction. *Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials*.

[29] S. Barraud *et al.*, "Performance of Omega-Shaped-Gate Silicon Nanowire MOSFET With Diameter Down to 8 nm," in *IEEE Electron Device Letters*, vol. 33, no. 11, pp. 1526-1528, Nov. 2012, doi: 10.1109/LED.2012.2212691.

[30] C. Mohan, Sumit .C and B. Prasad “Gate All Around FET: An Alternative of FinFET for Future Technology Nodes,” ICETETSM,vol.6,Jul.2017.

[31] J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes and C. Claeys, "Silicon-on-insulator 'gate-all-around device'," *International Technical Digest on Electron Devices*, San Francisco, CA, USA, 1990, pp. 595-598, doi: 10.1109/IEDM.1990.237128.

[32] Agarwal, A., Pradhan, P. C., and Swain, B. P. (2019). Effects of the physical parameter on gate all around FET. *Sadhana*, *44*(12). https://doi.org/10.1007/s12046-019-1232-8.

[33] W. Hu and F. Li, "Scaling Beyond 7nm Node: An Overview of Gate-All-Around FETs," *2021 9th International Symposium on Next Generation Electronics (ISNE)*, Changsha, China, 2021, pp. 1-6, doi: 10.1109/ISNE48910.2021.9493305.

[34] D. Jang *et al.*, "Device Exploration of NanoSheet Transistors for Sub-7-nm Technology Node," in *IEEE Transactions on Electron Devices*, vol. 64, no. 6, pp. 2707-2713, June 2017, doi: 10.1109/TED.2017.2695455.

[35] D. Yakimets *et al.*, "Vertical GAAFETs for the Ultimate CMOS Scaling," in *IEEE Transactions on Electron Devices*, vol. 62, no. 5, pp. 1433-1439, May 2015, doi: 10.1109/TED.2015.2414924.