Low-Power Three-Stage Dynamic Comparator with Tail Transistor Using 20-nm FinFET Technology for ADC Applications

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Abstract — Comparators are fundamental components in analog-to-digital converters (ADCs). The overall performance of an ADC strongly depends on the speed, power consumption, and accuracy of the comparator. Traditional CMOS-based comparators suffer from leakage current and short channel effects when implemented in deep submicron technologies. To address these challenges, this paper presents a three-stage dynamic comparator implemented using 20-nm FinFET technology. The proposed design incorporates a tail transistor in the latch stage to reduce power consumption and improve energy efficiency. The circuit was designed and simulated using Cadence Virtuoso with FinFET device models. Simulation results show significant improvement in power efficiency compared with conventional three-stage comparator architectures, making the proposed design suitable for high-speed and low-power ADC applications.

Keywords: FinFET, Dynamic Comparator, Analog-to-Digital Converter (ADC), Tail Transistor, Low Power Design

I. Introduction

Analog-to-digital converters are widely used in modern electronic systems such as wireless communication, biomedical devices, sensor systems, and embedded electronics. The comparator is one of the most important components in ADC architectures because it determines the decision speed and accuracy of the conversion process.

Dynamic comparators are commonly used due to their low static power consumption and high operating speed. However, conventional CMOS comparators experience performance degradation as device dimensions shrink. Problems such as leakage current, reduced voltage headroom, and short-channel effects limit their efficiency.

FinFET technology offers improved electrostatic control and reduced leakage current compared to planar CMOS devices. In this work, a three-stage dynamic comparator using 20-nm FinFET technology is proposed to enhance power efficiency and speed.

II. FinFET Technology Overview

FinFET (Fin Field Effect Transistor) is a multi-gate transistor structure that improves channel control in nanoscale technologies. The gate surrounds the channel from multiple sides, providing stronger electrostatic control compared with traditional planar MOSFETs.

The advantages of FinFET technology include reduced leakage current, higher drive current capability, improved switching speed, and better scalability. These properties make FinFET technology suitable for low-power high-performance VLSI circuits.

III. Conventional Dynamic Comparator

Dynamic comparators operate in three main phases: reset phase, amplification phase, and regeneration phase. During the reset phase, the internal nodes are precharged to defined voltage levels. In the amplification phase, the differential input voltage is amplified. During the regeneration phase, positive feedback in the latch stage quickly drives the output nodes to the supply rails.

Three-stage comparators use additional amplification stages to improve gain and reduce input referred noise. However, these additional stages may increase power consumption if the circuit is not properly optimized.

IV. Proposed Three-Stage Comparator with Tail Transistor

The proposed design introduces a tail transistor in the latch stage of the comparator. The main purpose of the tail transistor is to control the current flow between the supply and ground during different phases of operation.

When the clock signal is low, the tail transistor remains off, preventing current flow and reducing static power consumption. When the clock signal becomes high, the input differential signal is amplified and applied to the latch stage. The latch then regenerates the signal using positive feedback.

The addition of the tail transistor reduces unnecessary current paths and improves overall energy efficiency of the comparator.

V. Simulation Setup

The comparator circuit was implemented and simulated using Cadence Virtuoso simulation tools with 20-nm FinFET device models. Various performance parameters such as power consumption, delay, and energy efficiency were evaluated.

Simulation conditions:
Technology: 20 nm FinFET
Supply Voltage: 1 V
Input Voltage Difference: 1 mV to 100 mV
Simulation Tool: Cadence Virtuoso

VI. Results and Discussion

Simulation results show that the proposed comparator achieves lower power consumption compared to conventional three-stage comparators. The tail transistor reduces static current during the reset phase, resulting in improved energy efficiency.

The proposed design achieves approximately 20% reduction in power consumption while maintaining

acceptable propagation delay. These results demonstrate that the proposed architecture is suitable for low-power high-speed ADC applications.

VII. Circuit Architecture

Figure 1 shows the transistor level architecture of the proposed three-stage dynamic comparator with a tail transistor.

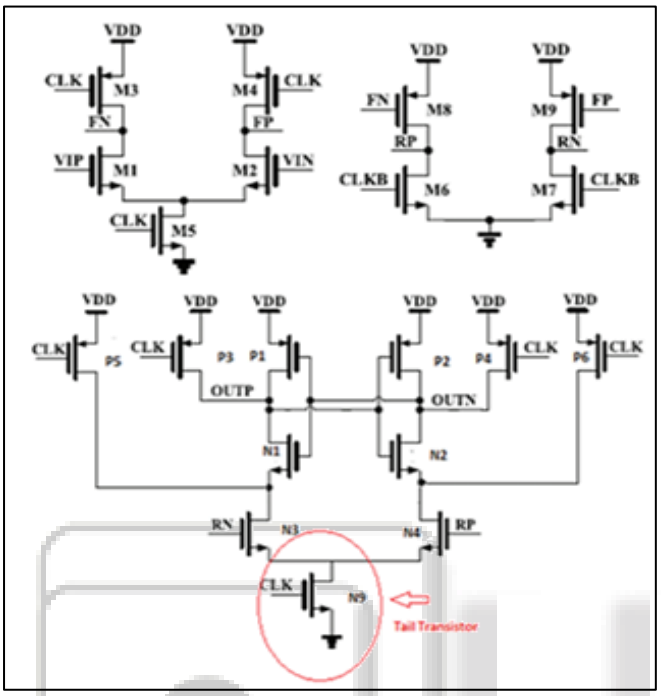

Fig.1 Transistor-level architecture of the proposed dynamic comparator with tail transistor.

VIII. Verilog Implementation

The behavior of the proposed comparator was modeled using Verilog HDL. The design consists of three stages: input comparison stage, regenerative stage, and output stage.

```
`timescale 1ns/1ps
module dynamic_comparator (
   input clk,
   input [7:0] vip,
   input [7:0] vin,
   output reg outp,
   output reg outn
);

reg stage1;
reg stage2;

// Stage 1 : Input comparison
always @(posedge clk)
begin
   if(vip > vin)
      stage1 = 1'b1;
   else
      stage1 = 1'b0;
end

// Stage 2 : Regenerative stage
always @(posedge clk)
begin
   stage2 = stage1;
end

// Stage 3 : Output stage
always @(posedge clk)
begin
   if(stage2)
   begin
      outp <= 1'b1;
      outn <= 1'b0;
   end
   else
   begin
      outp <= 1'b0;
      outn <= 1'b1;
   end
end

// Precharge phase
always @(negedge clk)
begin
   outp <= 1'b0;
   outn <= 1'b0;
end

endmodule
```

IX. Testbench and Simulation

A testbench was developed to verify the operation of the comparator using different input conditions.

```
`timescale 1ns/1ps
module comparator_tb;

reg clk;
reg [7:0] vip;
reg [7:0] vin;

wire outp;
wire outn;

dynamic_comparator DUT (
   .clk(clk),
   .vip(vip),
   .vin(vin),
   .outp(outp),
   .outn(outn)
);

// Clock generation
initial begin
   clk = 0;
   forever #5 clk = ~clk;
end

initial begin
   $dumpfile("dump.vcd");
```

```
    $dumpvars(0, comparator_tb);
end

initial begin
    vip = 8'd120; vin = 8'd100; #20;
    vip = 8'd50;  vin = 8'd150; #20;
    vip = 8'd200; vin = 8'd100; #20;
    vip = 8'd10;  vin = 8'd80;  #20;
    $finish;
end
endmodule
```

X. Simulation Waveforms

The simulation waveform obtained from EDA Playground verifies the correct operation of the comparator. When vip is greater than vin, the output outp becomes high and outn becomes low, otherwise the outputs switch accordingly.

Fig. 2: Verilog simulation waveform showing clock, input signals, intermediate stages, and comparator outputs.

XI. Conclusion

This paper presented the design of a low-power three-stage dynamic comparator using 20-nm FinFET technology. The inclusion of a tail transistor significantly reduces power consumption and improves energy efficiency.

The proposed comparator provides better performance compared with conventional architectures and is well suited for modern low-power ADC systems.

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