Performance Analysis of 19-Level Modular Cascaded MLI With Reduced Switch Count

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Abstract — Utility Multi-level inverters are increasing day-by-day in smart power system. With this their topologies are also evolving. The main challenge in designing the high-level inverters is to maintain efficiency and reliability with reduced component counts. Since as the level of output increases, requirement for the switches and other components like capacitor, diodes and sources also increases. This paper presents the cascaded type asymmetrical 19-level inverter with only 12 switches and four DC-sources. Asymmetrical topologies are the one which does not have any symmetry in the design and though the units are cascaded in structure, but they are different in topology. The proposed 19-level inverter is designed in MATLAB.

Keywords: Multilevel Inverters (MLI), Cascaded H-Bridge multi-level inverter (CHBMLI) Flying Capacitor MLI (FCMLI), Neutral Point Clamped (NPCMLI), Total Harmonic Distortion (THD).

I. INTRODUCTION

In many industrial and renewable energy applications these days, Multilevel Inverters (MLI) are receiving more attention. Multilevel inverters have better power quality features and lower Total Harmonic Distortion (THD) than their two-level competitors. Many industries employ the traditional MLI topologies, such as Cascading H-Bridge MLI (CHBMLI), Flying Capacitor MLI (FCMLI), and Neutral Point Clamped or Diode Clamped MLI (NPCMLI), for a variety of purposes. Lower power level MLI is used in grinding mills, pumps, conveyor belts, reactive power compensation, propulsion of marine systems, and turbine starters, among other applications. High power applications include HVDC transmission systems, solar PV generation systems, wind energy generation systems, and traction in railways. [1]–[4].

The fact that NPC and FC topologies only require a single isolated DC-source inside their structures is a significant benefit. However, they require additional switches, diodes, and capacitors in order to give an output with a bigger number of voltage levels. Neutral point balancing necessitates the use of an additional circuit, which is another disadvantage of the NPC and FC topologies. Many kinds of research have been done to address these problems, but the suggested designs are still plagued by a high number of devices in their structures [5,6]. MLIs have been designed with CHB-based topologies because of their simple controllability, simplicity of construction, and reduced number of capacitors. Rechargeable batteries, electrical vehicles, PV systems, reactive compensators, etc. have all made extensive use of them [7–10]. It is possible to configure the CHB-topology in an asymmetrical mode.

This paper also presents the reduced switch count topology of 19-level inverter using cascaded structure. In conventional cascaded structure for 19-level, 36 switches are required where as in the proposed structure only 12 switches are used to generate19-level output which is one third of the conventional topology. Also, in conventional topology each-unit required one DC-source. Therefore, in total eight sources where as in the proposed topology only four sources are required.

II. CASCADED H-BRIDGE MULTI-LEVEL INVERTER

The Cascaded H-Bridge multi-level inverter (CHBMLI) has been used in an extensive variety of uses in present days [11]. With its modularity and adaptability, the CHMLI demonstrates prevalence in high power and high voltage applications, particularly series and shunt connected FACTS controllers. The CHMLI gives its output voltage almost sinusoidal output voltage waveforms by joining numerous isolated (disengaged) voltage levels. The dc connection supply for every full bridge converter is given independently, and this is commonly accomplished utilizing diode rectifiers encouraged from the isolated secondary windings of a three-phase transformer.

The CHB-MLI topology is depends on the series arrangement of single-phase full bridge inverters with more number of dc links. Figure 1 shows the general schematic of the CHB-MLI with n- number of levels. A single phase full bridge (H-bridge) converter is capable to produce 3 different output voltage levels i.e. +Vdc, 0 and - Vdc. Each leg present in H-Bridge have two possible conducting states, to avoid dc-link capacitor short-circuit. The output phase voltage is analysed by summing of the output voltages of the all bridges [12, 13].

A. *Advantages:*

- This topology is simple and easy to control.
- The number of capacitors and other semiconductor devices are very less compared to other type of topologies.

B. *Disadvantages:*

- It requires separate DC-links or capacitors (batteries) for each module.
- Cost and complexity will increase for high level inverters because of the separate dc sources.

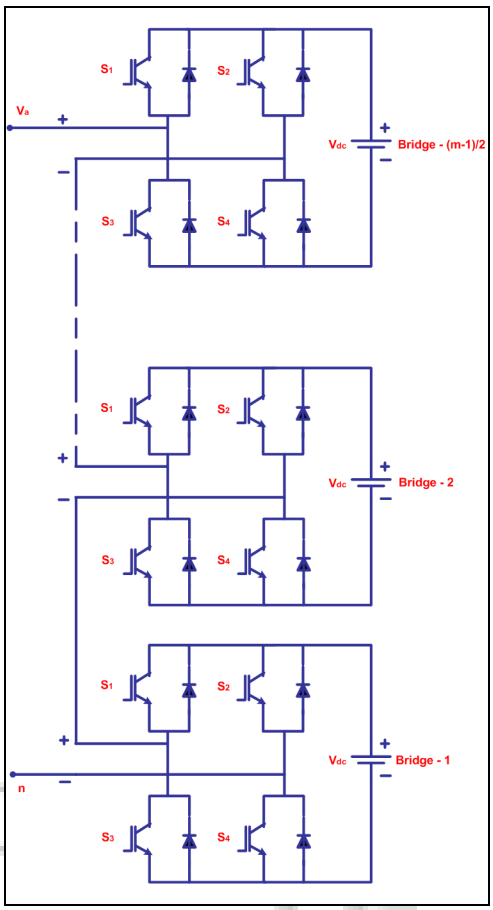


Fig. 1: Generalized structure of Cascaded MLI topology

III. PROPOSED WORK

In high-control applications the traditional square wave inverters have certain limits like high harmonics generation which results in power quality issues. In cutting edge years, Multilevel inverters have been used in medium and high power applications, for example, Flexible AC transmission System (FACTS), mechanical engine drives, footing electric vehicle applications, drive frameworks etc [14].

In this proposition, there is also an increase in trends for cross breed multi-level inverter for example in [15], flying capacitor inverter and cascaded H-connect models with drifting capacitors has been displayed, which is producing seventeen levels of yield voltage (shaft voltage). Furthermore, these hybrid inverters can produce a more strides of voltage levels with decreased number of switches, gate driver circuits and diodes as contrast with customary multilevel inverter. Another element of these inverters is its capacity to create the voltages from a solitary dc-interface control supply which empowers consecutive operation of converter [16, 17].

The output voltage waveform is nearly a sine wave with least harmonics, enhancing the execution of the drive exhibited in this theory as the quantity of voltage levels increments. The work depicted in this postulation produces distinctive voltage levels by exchanging the current through capacitors. Here, by taking the excess states for a similar shaft voltage, the bearing of load current through the capacitor can be changed.

This piece of work presents a lesser switch count 19 level inverter (19-LI) with circuit topology as shown in figure 2. Although the presented 19-LI resembles H-bridge, the inverter has less components than a conventional 19-level H-bridge inverter. It generates 19-level inverter with two symmetrical blocks and 4 different level DC sources. There are 12 switches in the current scheme. To examine the various voltages under load at different intervals, each of the 12 switches must receive a unique pulse. In conventional 19-level cascaded topology, for generating 19-level 36 switches are required. This work is also compared with the base paper which also proposes hybrid 19-level topology.

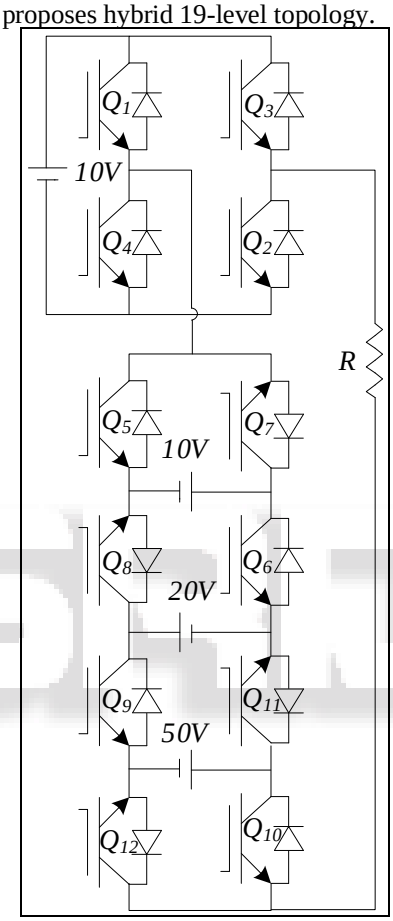


Fig. 2: Presented 19-LI

IV. SIMULATION RESULTS

The proposed system has been analysed in matlab simulation. The state-of the art-of any MLI is designing of its gate pulses, which controls the conduction of switches. In this work gate pulses are designed using sinusoidal carrier wave phase opposition disposition modulation. For generating nineteen level, 18 input signals in the form of triangular pulse generator is used where as 1 sine wave as a carrier signal is used as shown in figure 3. The paper proposed asymmetrical 19-level inverter is analysed for constant resistive load of 300 Ω. The simulation parameters are shown in table-1.

Parameters	Value
Number of level	19
Voltage level	160 V
No. of DC-source	4 (18 V, 18V, 36 V, 90 V)
No. of switches	12
No. of diodes	Nil

No. of Capacitors	Nil
Sample Time	50 µs
Switching frequency	5 kHz
Output frequency	50 Hz
Resistive load	R = 300 Ω
THD	0.94%

Table 1: Design Parameter

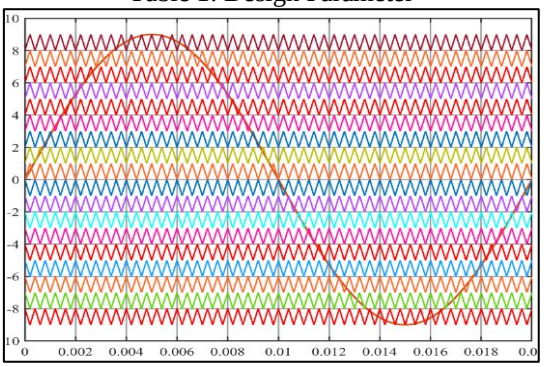


Fig. 3: Phase opposite level shift deployed PWM scheme

The output voltage and current for constant linear load is shown in figure 4 and figure 5 respectively. The harmonic analysis to verify the performance of the proposed topology is shown in figure 6 having 0.94% THD, hence no filter is required to reduce the harmonic. The voltage and current across each switches are shown in figure 7- figure 18 for all the 12 switches sequentially.

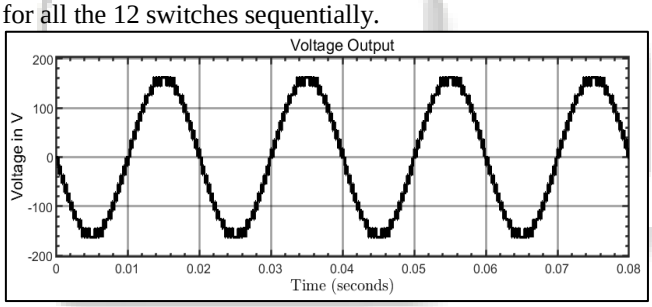


Fig. 4: Output voltage of proposed 19-level inverter

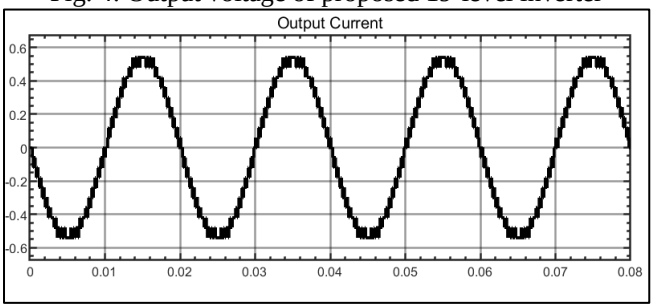
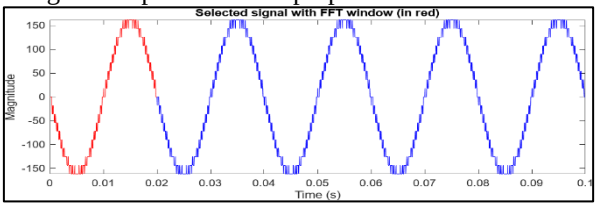


Fig. 5: Output current of proposed 19-level inverter



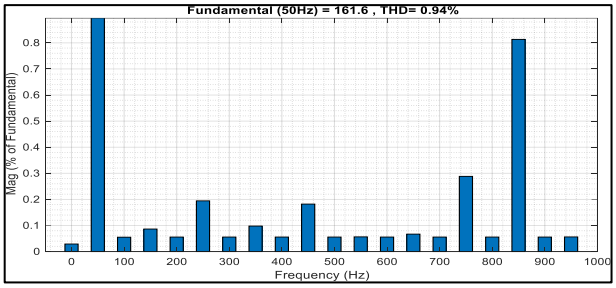


Fig. 6: THD Profile

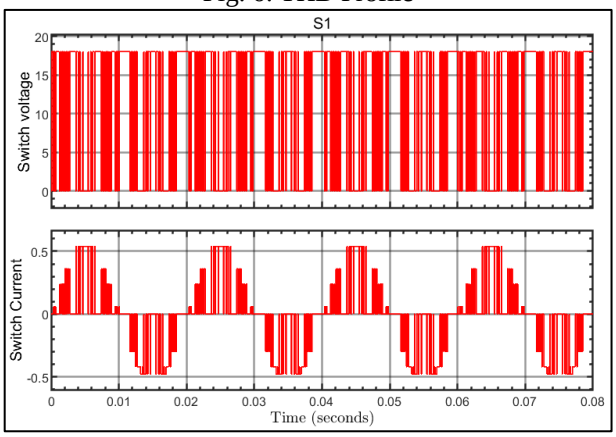


Fig. 7: Voltage and current for switch 1 (S_1)

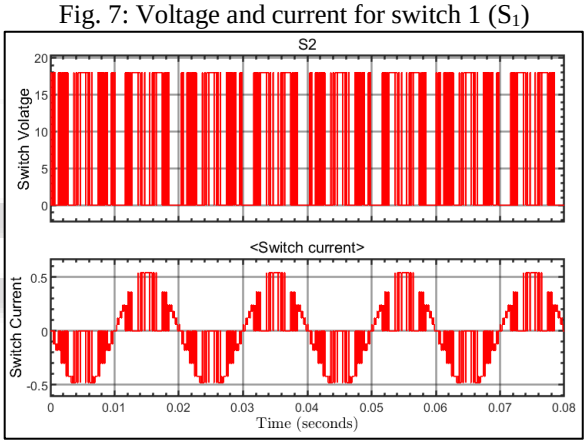


Fig. 8: Voltage and current for switch 2 (S_2)

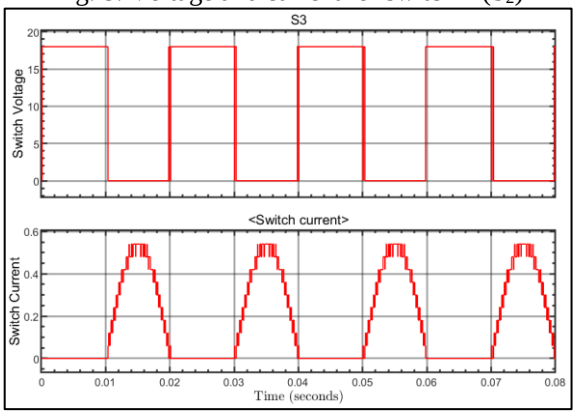


Fig. 9: Voltage and current for switch 3 (S_3)

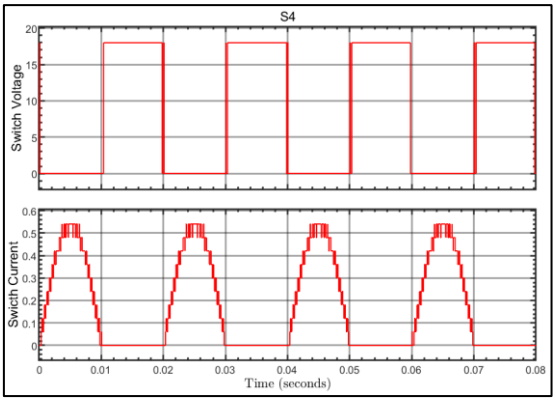


Fig. 10: Voltage and current for switch 4 (S_4)

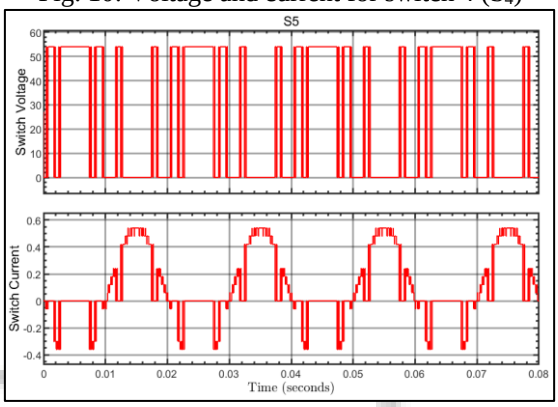


Fig. 11: Voltage and current for switch 5 (S_5)

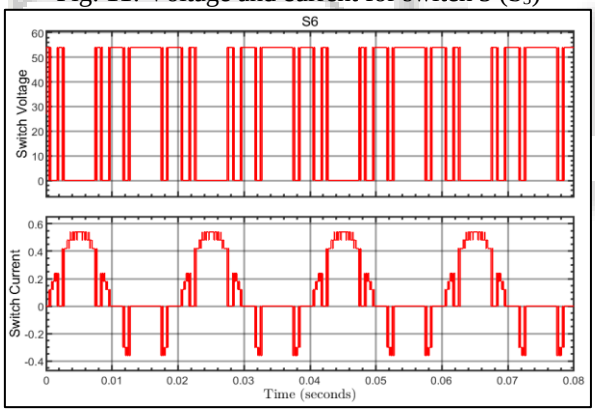


Fig. 12: Voltage and current for switch 6 (S_6)

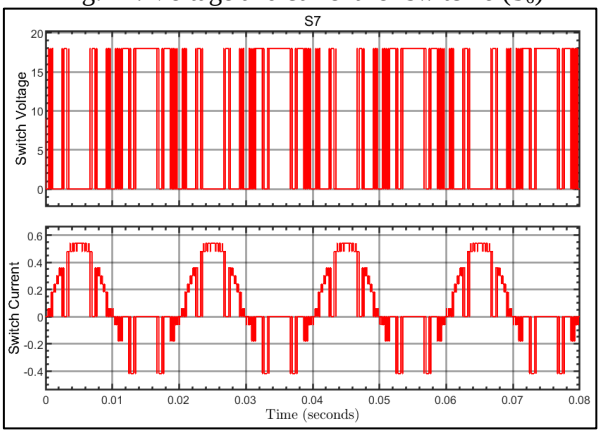


Fig. 13: Voltage and current for switch 7 (S_7)

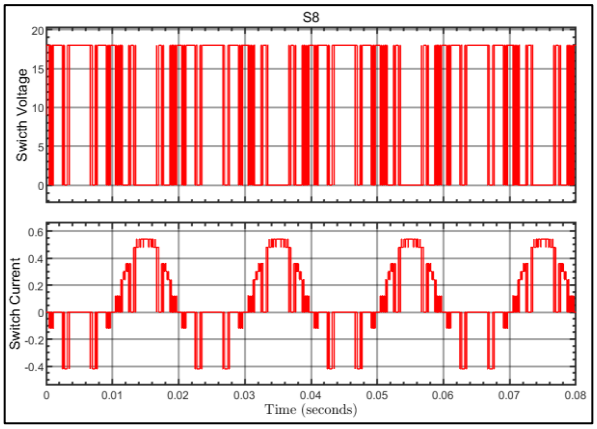


Fig. 14: Voltage and current for switch 8 (S_8)

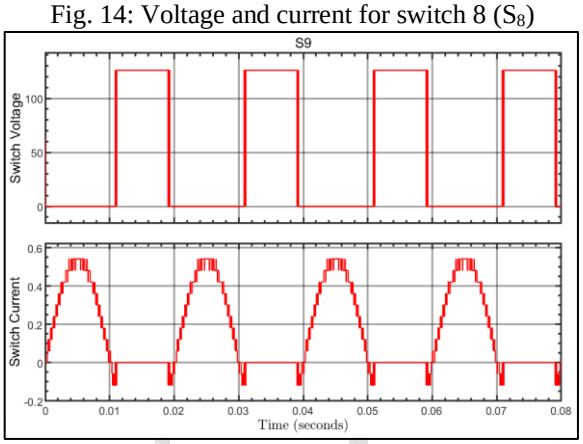


Fig. 15: Voltage and current for switch 2 (S_9)

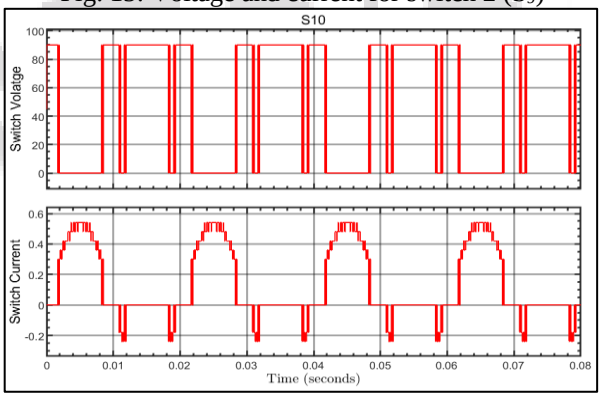


Fig. 16: Voltage and current for switch 10 (S_{10})

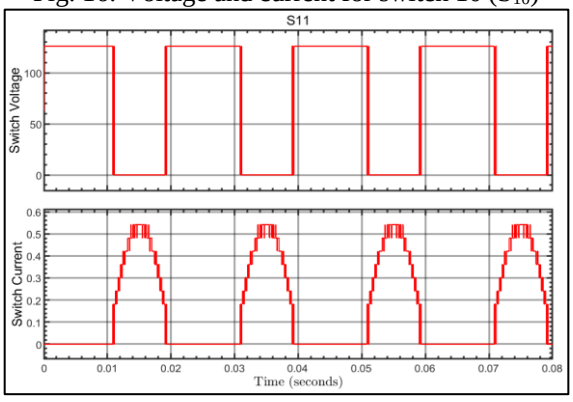


Fig. 17: Voltage and current for switch 11 (S_{11})

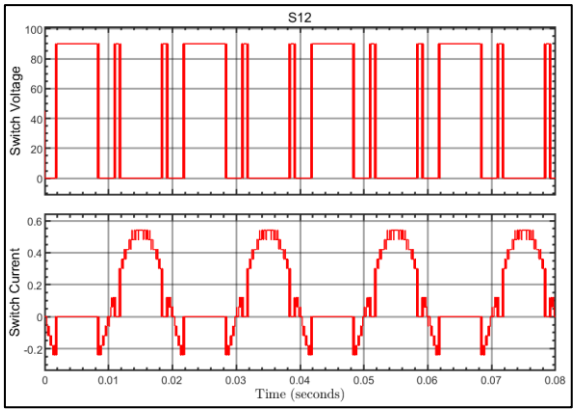


Fig. 18: Voltage and current for switch 12 (S_{12})

V. CONCLUSIONS

This paper presents the asymmetrical 19-level inverter using modular cascaded topology. the output wave form obtained has very small step size which replicate the sine wave, hence harmonic in the voltage wave is 0.94%. Since the harmonics are below the prescribed limit of IEEE standard for distribution system which is below 8%. The proposed 19-level inverter is efficient and can be used for very precise applications since it will maintain the quality of the DC-source.

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