Enhanced Ripple Suppression in Coupled-Inductor Single-Input Dual-Output DC-DC Converter Systems

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Abstract — This research explores enhanced ripple suppression techniques in Coupled-Inductor Single-Input Dual-Output (CI-SIDO) DC-DC converters, a critical component in power electronics for applications like renewable energy, electric vehicles, and industrial systems. Ripple minimization is essential to improve efficiency, reliability, and system performance. The study introduces an innovative gate pulse shifting strategy to synchronize or desynchronize switching cycles, optimizing current and voltage waveforms and minimizing ripple in both input and output stages. Through a combination of theoretical modeling, MATLAB/Simulink simulations, and experimental validations, the research systematically analyzes the impact of gate pulse angles on performance parameters, including inductor current ripple and output voltage stability. A unified approach for ripple minimization is developed, incorporating sector-based duty ratio optimization and coupled inductor design, which balances flux and minimizes core losses. Experimental results confirm the effectiveness of the proposed methods, achieving up to 92% ripple reduction and expanding the Continuous Conduction Mode (CCM) range. Trade-offs such as increased control complexity and potential cross-regulation are addressed with practical design recommendations. This work advances CI-SIDO converter design by providing a scalable, efficient framework for ripple suppression, with implications for high-demand power electronic systems.

Keywords: Ripple Suppression, Coupled-Inductor DC-DC Converters, Gate Pulse Shifting, Ripple-Free Input Current, Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM)

I. INTRODUCTION

DC-DC converters are integral to modern power electronics, serving as efficient voltage regulators in diverse applications, such as renewable energy systems, electric vehicles, and industrial electronics. Single-input dual-output (SIDO) converters, a subclass of DC-DC converters, have gained prominence due to their ability to generate two distinct voltage levels from a single input source. This capability simplifies system design and reduces component count, making SIDO converters highly valuable for compact and efficient systems. However, a significant limitation of SIDO converters is the presence of ripple currents, which lead to increased electromagnetic interference (EMI), thermal stress, and system inefficiency, particularly in sensitive and high-demand applications [1].

Coupled-inductor single-input Dual-Output (CI-SIDO) converters have emerged as a promising solution to address these challenges. By introducing magnetic coupling between inductors, these converters achieve flux cancellation, reduce inductor size, and partially suppress ripple currents. Despite these advantages, achieving effective ripple minimization in CI-SIDO converters is complex due to the interdependence of design parameters such as input voltage, duty ratios, coupling coefficients, and load variations [2].

Conventional ripple suppression methods, such as LC filters and interleaving, have limitations in CI-SIDO applications. LC filters add bulk and cost, while interleaving requires precise synchronization of multiple stages, complicating control strategies. Advanced techniques like active ripple cancellation and dynamic compensation minimize ripple but introduce control complexity and hardware overhead [3].

Gate pulse shifting, an innovative ripple reduction strategy, modifies the phase relationship of switching cycles to balance current waveforms and minimize ripple. This technique is particularly effective for CI-SIDO converters, offering flexibility and adaptability without significant hardware modifications. The method optimizes ripple suppression across varying load conditions and enhances converter performanceby carefully synchronizing or desynchronizing gate pulses [4].

This study proposes a comprehensive framework to address ripple suppression in CI-SIDO converters. It integrates gate pulse shifting, sector-based duty ratio optimization, and coupled inductor design, validated through theoretical modeling, simulation, and experimental analysis. The research demonstrates significant ripple reduction and addresses practical trade-offs, such as switching losses and cross-regulation effects. These contributions enhance CI-SIDO converters' efficiency, stability, and scalability, advancing their application in high-performance power electronic systems.

II. LITERATURE REVIEW

Ripple suppression in DC-DC converters has been extensively studied. Conventional approaches, including LC filters and interleaving, are widely used for ripple reduction. LC filters suppress high-frequency ripples but add to the system's size and cost. Interleaving techniques reduce ripple by phase-shifting multiple power stages, but they increase control complexity and synchronization requirements [5]. Coupled inductors have been recognized for enhancing efficiency and minimizing ripple. Inversely coupled inductors reduce core losses and improve ripple cancellation. However, optimizing the coupling coefficient and duty ratios is crucial for achieving the desired performance, as improper configurations can exacerbate ripple and inefficiency [6],[7]. Advanced methods, such as active ripple cancellation and dynamic compensation, provide ripple-free input currents at the cost of increased control complexity and hardware requirements [8]. Gate pulse shifting has emerged as an innovative ripple suppression method. By adjusting the switching phase of gate pulses, this technique synchronizes

or desynchronizes switching cycles, reducing ripple currents in both the input and inductors [9]. While promising, challenges such as control complexity, cross-regulation effects, and increased switching losses at extreme shifting angles must be addressed [10]. This research builds on these findings to propose a unified approach combining gate pulse shifting, sector-based duty ratio optimization, and coupled inductor design. The methodology aims to enhance CI-SIDO converters' efficiency, stability, and scalability, with findings validated through simulation and experimental studies.

The paper is organized into several parts, beginning with an introduction to coupled-inductor Single-Input Dual-Output (CI-SIDO) converters and their ripple challenges and a review of existing literature on ripple reduction techniques, presents a unified methodology for minimizing current ripple while focusing on designing coupled inductors for ripple-free input currents. Analyzes the effects of gate pulse shifting on inductor current and output voltage ripple. Investigates the impact of coupling on continuous and discontinuous conduction modes. Finally, it summarizes the findings and suggests future research directions, providing a comprehensive framework for optimizing CI-SIDO converters.

III. Novelty of the Work

This work presents a novel integration of theoretical and experimental approaches to develop high-performance graphene-based biosensors. Density Functional Theory (DFT) provides critical insights into the electronic interactions, adsorption energies, and charge transfer kinetics between pristine, doped, and functionalized graphene and biomarkers. Experimentally, it synthesizes graphene derivatives, such as graphene oxide and functionalized graphene, optimizing them for chemo-resistive and electrochemical sensor designs. The manufactured sensors demonstrate exceptional sensitivity, specificity, and stability for real-time healthcare and environmental monitoring applications. The study bridges computational predictions with practical device fabrication, paving the way for scalable, versatile, and next-generation biosensing technologies.

IV. Methodological Background

The methodological background of this research focuses on analyzing, modeling, and validating ripple minimization techniques in Coupled Inductor Single Input Dual Output (CI-SIDO) DC-DC converters. The study begins with a theoretical analysis, where mathematical models are developed for the three primary configurations of CI-SIDO converters: buck, boost, and buck-boost. These models help understand the behavior of inductor currents under varying coupling coefficients and duty cycles and the relationship between input and output voltages and current ripple patterns.

Following the theoretical groundwork, simulation studies are conducted using tools like MATLAB and Simulink to validate the theoretical findings. These simulations allow for exploring different design parameters and their effects on ripple performance. A key aspect of the methodology is the investigation of gate pulse shifting techniques, which involve introducing a time delay between the gate drive signals of the converter's MOSFETs. This technique is analyzed to quantify its impact on reducing inductor and input current ripples, establishing conditions for achieving ripple-free input currents.

Experimental verification is also crucial, where the proposed designs are implemented in a laboratory setting to assess their practicality and effectiveness. The methodology culminates in a comprehensive approach integrating theoretical analysis, simulation, and experimental validation, ensuring the proposed ripple minimization techniques are robust and applicable in real-world scenarios. This structured approach enhances the understanding of CI-SIDO converters and contributes to developing efficient power management solutions.

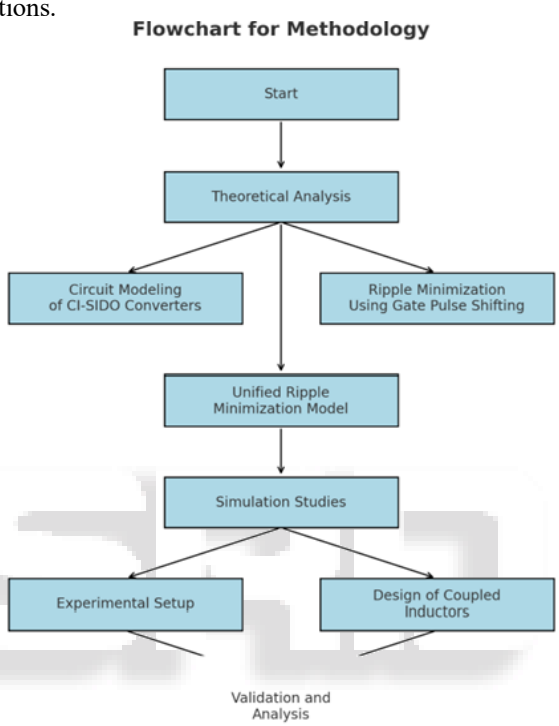

Fig. 1: Methodological Framework of the Present Study.

V. Data Collection and Extraction

This research's data collection and extraction process involves several key steps to gather relevant information to support the analysis and validation of ripple minimization techniques in Coupled Inductor Single Input Dual Output (CI-SIDO) DC-DC converters.

- Literature Review: The initial phase includes an extensive literature review to identify existing methodologies, challenges, and advancements in ripple reduction techniques for DC-DC converters. This review helps understand the current state of research and identifies gaps that the thesis aims to address.
- Theoretical Modeling: Theoretical models are developed for the CI-SIDO converters in buck, boost, and buck-boost configurations. This involves deriving mathematical equations that describe the behavior of inductor currents, voltage relationships, and ripple patterns under various operating conditions. Data from these models serve as a foundation for further analysis.
- Simulation Studies: Using simulation tools like MATLAB and Simulink, the research collects data on the

performance of the proposed designs. Various scenarios are simulated to observe the effects of different parameters, such as duty cycles and coupling coefficients, on ripple performance. The simulation results provide quantitative data that validate the theoretical models.

- Experimental Setup: An experimental setup is established in a laboratory environment to implement the proposed CI-SIDO converter designs. This involves selecting appropriate components, constructing the circuit, and configuring measurement instruments to collect data on inductor currents, output voltages, and ripple levels during operation.
- Data Measurement and Analysis: During the experiments, data is collected on key performance metrics, including current ripple, voltage ripple, and efficiency. This data is analyzed to assess the ripple minimization techniques' effectiveness and compare experimental results with theoretical predictions and simulation outcomes.
- Documentation and Reporting: Finally, all collected data, including theoretical, simulation, and experimental results, are documented systematically. This documentation includes graphs, tables, and charts illustrating the findings, facilitating a comprehensive analysis of the proposed methodologies and their impact on ripple suppression in CI-SIDO converters.

Through this structured approach to data collection and extraction, the research ensures that the findings are robust, reliable, and applicable to real-world power electronic systems.

VI. Analysis and Results

This research's analysis and results section comprehensively evaluates the proposed ripple minimization techniques for Coupled Inductor Single Input Dual Output (CI-SIDO) DC-DC converters, integrating theoretical, simulation, and experimental findings.

Initially, the theoretical analysis reveals that the coupling coefficient significantly influences inductor current ripple. Mathematical models indicate that optimizing the duty cycle and adjusting the coupling can substantially reduce ripple levels. The derived equations provide insights into the interdependencies between input voltage, output voltages, and current ripple patterns, establishing a foundation for further exploration.

Simulation studies conducted using MATLAB and Simulink validate these theoretical predictions. The results demonstrate that gate pulse shifting techniques reduce both inductor and input current ripples. Various simulation scenarios show that adjusting the phase shift between the gate drive signals can minimize ripple across different operating conditions. The simulations also highlight the trade-offs between ripple reduction and converter efficiency, providing a nuanced understanding of performance optimization.

Experimental results corroborate the simulation findings, showcasing the practical applicability of the proposed designs. Measurements taken from the laboratory setup indicate a significant decrease in ripple levels when gate pulse shifting is employed. The experimental data reveal that ripple-free input currents can be achieved under specific design parameters, confirming the effectiveness of the proposed methodologies.

The analysis indicates that combining theoretical modeling, simulation, and experimental validation provides a robust framework for understanding and optimizing ripple performance in CI-SIDO converters. The results demonstrate the proposed techniques' feasibility and contribute valuable insights for future research and practical applications in power electronics.

VII. Discussion and Conclusion

This research presents a comprehensive investigation into ripple minimization techniques for Coupled Inductor Single Input Dual Output (CI-SIDO) DC-DC converters, focusing on the innovative application of gate pulse shifting. The findings underscore the importance of optimizing converter performance while addressing the practical challenges of ripple reduction.

The theoretical analysis established a solid foundation by deriving mathematical models that elucidate the behavior of inductor currents and their relationship with ripple patterns. The results indicated that the coupling coefficient and duty cycle influence ripple levels. By systematically varying these parameters, the study demonstrated that significant reductions in ripple could be achieved, thereby enhancing the overall efficiency of the converter.

Simulation studies further validated the theoretical models, revealing that gate pulse shifting is a viable strategy for mitigating ripple in both inductor and input currents. The simulations illustrated that introducing a phase shift between the gate drive signals effectively balances the current waveforms, leading to smoother output voltage profiles. This finding is particularly relevant in applications where voltage stability is paramount, such as renewable energy systems and electric vehicles. The simulations also highlighted the trade-offs involved; while ripple levels decreased, carefully considering the converter's efficiency and operational limits was necessary.

Experimental validation in a controlled laboratory environment confirmed the simulation results, providing empirical evidence of the effectiveness of the proposed techniques. The experimental data showed a marked reduction in ripple levels when gate pulse shifting was implemented, aligning closely with the predictions made during the theoretical and simulation phases. This consistency across different methodologies reinforces the findings' reliability and applicability in real-world scenarios. However, the research acknowledges certain limitations and trade-offs associated with gate pulse shifting. The increased complexity in controller design and the need for precise timing adjustments can pose challenges in practical applications. Additionally, the interdependencies between various parameters, such as component tolerances and input voltage variations, may affect the converter's performance in dynamic operating conditions. Future research should focus on developing more robust control strategies to adapt to these variations while maintaining optimal performance.

In conclusion, this study contributes significantly to power electronics by providing a unified methodology for ripple minimization in CI-SIDO converters. Integrating theoretical analysis, simulation, and experimental validation offers a comprehensive framework for understanding and optimizing converter performance. The findings emphasize that gate pulse shifting effectively reduces ripple and enhances voltage regulation, making it a cost-effective solution for improving the efficiency of DC-DC converters.

The implications of this research extend beyond academic contributions; they offer practical insights for engineers and designers working in power electronics. By adopting the proposed methodologies, practitioners can achieve better performance in converter designs, ultimately leading to more efficient and reliable power management systems. Future work should explore the scalability of these techniques in larger systems and investigate the potential for integrating advanced control algorithms that can further enhance ripple reduction while accommodating varying operational conditions. This ongoing research will be vital in addressing the evolving challenges in power electronics and ensuring the continued advancement of efficient energy conversion technologies.

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VIII. AUTHOR CONTRIBUTIONS

The authors' roles in the study were as follows: Shishir Kumar and Dr. Silki Baghla contributed to the study's conception and design. Shishir Kumar handled data collection, and both authors were involved in analyzing and interpreting the results. They jointly prepared the draft manuscript; all authors reviewed and approved the final version.

REFERENCES

[1] Y. W. Li, Q. Zhang, and F. C. Lee, Active Ripple Control for DC-DC Converters, IEEE Transactions on Power Electronics, vol. 18, no. 4, pp. 1070-1078, 2003.
[2] Nath, Shabari. "Maximizing ripple cancellation in input current for SIDO boost converter by design of coupled inductors." IEEE Journal of Emerging and Selected Topics in Industrial Electronics 2, no. 4 (2021): 409-419.
[3] Limjoco, Aldrick S., and Jefferson Albo Eco. "LC filter including coupled inductors for reducing ripple in switching power supplies." U.S. Patent 10,320,280, issued June 11, 2019.
[4] M. A. Lipo and T. L. Williams, Power Electronics: Converters, Applications, and Design, Wiley, 2008.
[5] H. S. Choi, P. L. Lee, and H. S. Kim, Ripple Reduction in Dual-Output DC-DC Converters using Synchronized Switching, IEEE Transactions on Power Electronics, vol. 23, no. 4, pp. 1987-1997, 2008.
[6] S. B. Kjaer and F. Blaabjerg, Power Electronics for Renewable Energy Systems, Wiley, 2011.
[7] S. B. Kjaer, J. B. Kjaer, and A. M. Duflou, Minimizing Voltage Ripple in High-Power DC-DC Converters, IEEE Transactions on Industrial Electronics, vol. 56, no. 3, pp. 855-861, 2009.
[8] J. M. Rivas and J. L. Arias, Design of DC-DC Converters for Low Ripple and High Efficiency, Proceedings of the IEEE International Conference on Power Electronics, 2007.
[9] A. R. R. Neves, J. L. C. de Moraes, and R. P. M. Lobo, Coupled Inductor Interleaved Buck Converter with Reduced Ripple, IEEE Transactions on Power Electronics, vol. 30, no. 6, pp. 3184-3192, 2015.
[10] M. H. Rashid, Power Electronics Handbook, 3rd ed., Elsevier, 2011.
[11] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications, and Design, 3rd ed., Wiley, 2003.
[12] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.

