

Study and Implementation of Band Gap Reference Circuit for Constant Voltage Generation using Foundry Based MOS models

Rishabh Singh¹ Ritik Bharadwaj² Prince Divedi³ Harshit Chaturvedi⁴

^{1,2,3,4}Department of Electronics & Communication Engineering

^{1,2,3,4}ABES Institute of Technology, Ghaziabad, Uttar Pradesh, India

Abstract— This study deals with the design of BGR Circuit. Also detailed analysis of Foundry based MOSFET/BJT models will be done and shown in this work to give an insight on their characteristics. The BGR Circuit will consist of a current reference and generation Circuit, a PTAT and CTAT components which basically are Resistor and diode connected BJT respectively. The design will use the Sub-micron technology model of 45nm CMOS Process. Later in the end this work will show the generation of Voltage which is PVT invariant and constant and corresponds to Bandgap of Semiconductor device which intrinsic property of the same.

Keywords: Dolomite Powder, Compressive Strength, Split Tensile Strength, Flexural Strength

I. INTRODUCTION

Bandgap voltage reference is a temperature independent voltage reference circuit widely used in integrated circuits [7]. Bandgap reference (BGR) circuits are widely used in modern LSIs to generate a reference voltage on chips [6]. It produces a fixed (constant) voltage regardless of power supply variations, temperature changes, or circuit loading from a device. It commonly has an output voltage of 1.25 V (close to the theoretical 1.22 eV band gap of silicon). Reference voltage Generators are used in DRAM's, Flash Memories and analog devices. This generator is necessary to stabilize the over process, voltage and temperature variations [1] by Shigeru Atsumi. In the conventional implementation of Bandgap voltage reference generates an output voltage equal to 1.25V which is measured in electron volts. It cannot be used in latest deep-submicron technologies. BGR circuits, was designed either be required an external power on reset signal or to be composed of several MOS transistors for generating bias current, and the bandgap core circuit has two nodes that are controlled currents and voltages by resistors of the same value for generating the CTAT and PTAT currents [5].

Moore's Law is only applied or possible when the size of the transistor decreases exponentially over time. In 1965, Gordon Moore observed that the number of transistors in a chip increased exponentially over time. When he predicted this the size of the transistor was 100 μ m [2] according to S. E. Thompson. There are many types of these circuits in the state of the art, being the bandgap voltage reference (BGR) circuit the most popular since it can provide a predictable output voltage. [3] by E. Vilella

In this paper, we described about the transistor structure used in a 45-nm generation CMOS logic technology compared with 180-nm CMOS technology designed for high speed and low power operation and all CMOS bandgap voltage reference circuit which is designed with a new startup circuit for self - biased op-amp by using only one NMOS transistor and the bandgap core circuit is designed by defining the current and voltage with only one node and another node

set equal voltage which can be controlled by input voltages of op-amp.

A voltage reference is a simple block which remains constant against variation in operating voltage and temperature Fluctuations [4]. This method is able to reduce number of the resistor with a circuit solution suitable for low supply voltage operation and achieve the correct biased point at power on and successfully operate with near 1V supply voltage.

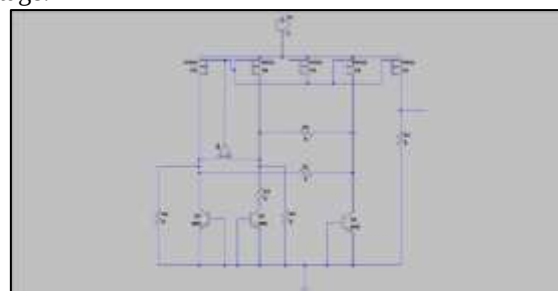


Fig. I: Architecture of Curvature Corrected BGR

II. NEED FOR REFERENCE

The integrated circuit should work at all temperature zones like desert and polar region. We need a reference voltage independent of temperature so that we can compare it with another voltage that is dependent of temperature and we can display how much is the actual temperature.

The reference should be independent of PVT variations: -

P – Process: We have IC's fabricated on different processors such as: CMOS 130nm, 65nm etc.

V – Supply Voltage

T – Temperature: It should lies b/w -40 to 125 degree Celsius

Parameter	Value @ VDD=1.3V	Unit
Temp Range	-40 $\rightarrow$ 125	$^{\circ}$ C
Vref @ 27 $^{\circ}$ C	1.113	V
Max Δ Vref	49	mV
Power Consumption	213.1	μ

Table I. Component Values of the BGR and Start up Circuit

III. GENERATING BGR ON CHIP

We need to identify CTAT and PTAT in the given circuit diagram.

We have (V_{be}) as a CTAT voltage at positive terminal that will reduced w.r.t to temperature at a rate of -2mV/c. The constant current source (I_1) is given. V_T as Thermal voltage is a PTAT as whenever the temperature increases the voltage will also increases at a rate of +0.085mV/c. We have multiply it with some number say M so that the slope will increase to +2mV/c. After that we will get the temperature independent reference which is a constant and sum it to get the output result BGR as:

$$\rightarrow V_{out} = V_{be} + M V_T$$

IV. CTAT CIRCUIT

The voltage across a diode operated at constant current is *complementary to absolute temperature (CTAT)*, with a temperature coefficient of approximately -2 mV/K .

In the circuit, we have a current source connected between Vdd and BJT which is a diode connector whenever collector and base are shorted and Vbe is Q1 which represents the CTAT behavior.

V. PTAT CIRCUIT

The voltage difference between two p-n junctions (e.g. diodes), operated at different current densities, is used to generate a current that is *proportional to absolute temperature (PTAT)* in a resistor. This current is used to generate a voltage in a second resistor.

In the circuit,

Now suppose we have 2 circuits with current source Ic in which first circuit has one transistor A and another circuit has n transistors nA.

$$\rightarrow V_{be} = V_t \ln(I_c/I_s) \quad \text{--- (1)eqn.}$$

The above equation is used to find the vbe for both circuits. The first circuit with one transistor A will be written as:

$$\rightarrow V_{be1} = V_t \ln(I_c/I_s) \quad \text{--- (2)eqn.}$$

The second circuit with n transistors nA will be written as:

$$\rightarrow V_{be2} = V_t \ln(I_c/n / I_s) \quad \text{--- (3)eqn.}$$

Taking difference of (2) and (3) eqn. we will get PTAT quantity:

$$\rightarrow V_{be1} - V_{be2} = V_t \ln(n)$$

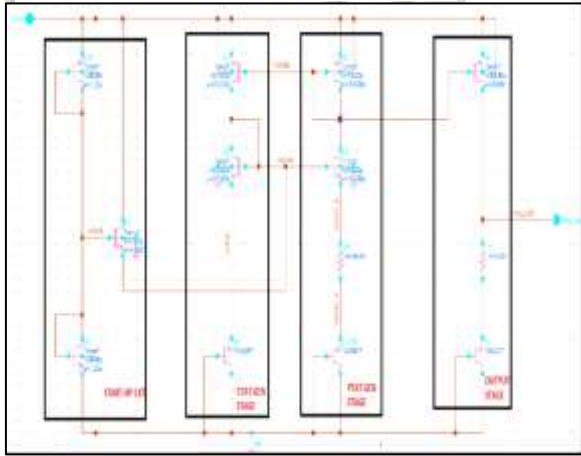


Fig. II: Combined CTAT and PTAT

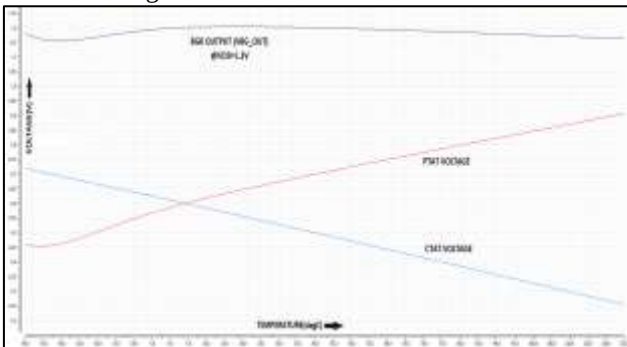


Fig. III. BGR Output Waveform Circuit for CTAT and PTAT

VI. BGR CIRCUIT

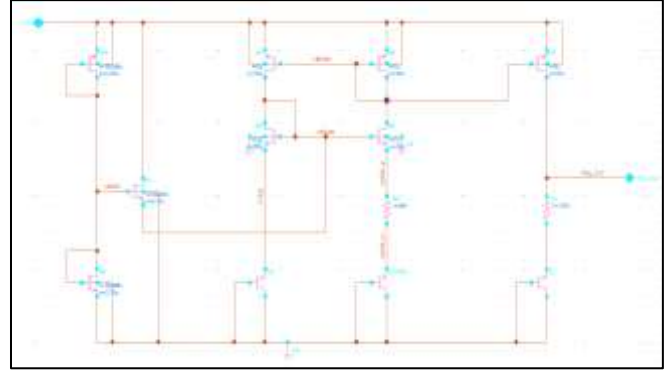


Fig. IV: Final Circuit 45nm

We know that,

$$\rightarrow V_{be1} - V_{be2} = V_t \ln(n)$$

Here we have circuit using an OP-AMP. We will write Vbe1 at one transistor and because of virtual ground whatever voltage will be at one terminal same voltage will go on another terminal when the output gain is high. Therefore, at positive terminal it is Vbe1.

Now voltage across R1 will be:

$$\rightarrow V_{R1} = V_{be1} - V_{be2} = V_t \ln(n)$$

Which is also called as PTAT voltage and Vbe2 is CTAT voltage.

At the moment, $V_{bgr} = V_{be2} + V_t \ln(n)$

$\ln(n)$ should be 23 so that we multiply it with CTAT to get $+2 \text{ mV/c}$

$$V_{be2} + V_t (2) [11]$$

Then,

$$\rightarrow V_t \ln(n) / R_1 * R_2$$

So,

$$\rightarrow V_{bgr} = V_{be2} + V_t \ln(n) + V_t \ln(n) / R_1 * R_2$$

$$\rightarrow V_{bgr} = V_{be2} + V_t \ln(n) [1 + R_2/R_1]$$

$V_{bgr} = V_{CTAT}$

Finally, we can understand that,

$$\rightarrow V_{bgr} = V_{be1} + V_t \ln(n) R_2/R_1$$

Instances	Design Parameters
M10, M6, M7	W/L=1.25u/0.09u
M0, M1, M2, M3, M9	W/L=18u/0.36u
R0	0.44K
R1	14.28K
m	2

Table II: Electrical Characteristics of the Proposed Circuit

VII. CONCLUSION

The design or layout of a new radiation-tolerant temperature compensated BGR circuit in a standard 45nm CMOS technology is proposed. To afford powering at 1.3V, the trimming system based on resistors that enables multiple voltage operation modes within the same circuit introduced by this design. Radiation tolerance is achieved through the use of enclosed nMOS transistors and guard rings. Post-layout simulations for a temperature range of -40°C to 125°C are presented, showing that the new circuit is capable of working properly with either 1V and 1.3V supply voltages. Further characterization will be performed after the fabrication of the circuit.

REFERENCES

- [1] Shigeru Atsumi "A CMOS Bandgap Reference Circuit with Sub-1-V Operation", IEEE Journal of Solid-State Circuits, VOL. 34, NO. 5, pp. 670-674, 5 May 1999.
- [2] Scott E. Thompson "A 90-nm Logic Technology Featuring Strained-Silicon", IEEE Transactions Electronic Devices, VOL. 51, NO. 11, pp. 1790-1797, November 2004.
- [3] E. Vilella "Design of a Bandgap Reference Circuit with Trimming for Operation at Multiple Voltages and Tolerant to Radiation in 90nm CMOS Technology", IEEE Annual Symposium on VLSI, pp.269-272, 2010.
- [4] Miss Rohini Hongal "Design and Implementation of Curvature Corrected Bandgap Voltage Reference-1.1v using 180nm Technology", IEEE Annual Symposium on VLSI, pp. 294-299, 2010.
- [5] Saweth HONGPRASIT "Design of Bandgap Core and Startup Circuits for All CMOS Bandgap Voltage Reference", Przegląd Elektrotechniczny (Electrical Review), pp. 277-280, 2012.
- [6] Yuji Osaki "1.2-V Supply, 100-nW, 1.09-V Bandgap And 0.7-V Supply, 52.5-nW, 0.55-V Sub bandgap Reference Circuits for Nanowatt CMOS LSIs" IEEE Journal of Solid-State Circuits, Vol. 48, NO. 6, pp. 1530-1538, 6 June 2013.
- [7] Anjani Kumar Singh "A Wide Temperature Range Voltage Bandgap Reference Generator in 32nm CMOS Technology", Proceedings of 201 Global Conference on Communication Technologies (GCCT 2015), pp. 696-699, 2015.

