Design of Three Stage Dynamic Comparator with Tail Transistor using 20nm FinFET Modified to Transmission Gate Based Clock Gating Technique

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Abstract— According to this article, one of the key disadvantages is excessive power consumption and offset in CMOS based comparators. At scale down technology, CMOS suffers with short channel effect and leakage current. To address these challenges, FinFET technology is used in three stage dynamic comparators instead of traditional circuit designs. The energy efficiency of FinFET-based dynamic comparators is higher than that of CMOS, and the short channel effect and leakage current are decreased. Furthermore, a new design of FinFET-based three stage dynamic comparators with tail transistors was created and simulated using the cadence virtuoso environment. In this paper, A three stage comparator is presented in a novel architecture. The methodology used for this architecture is Clock Gating technique. In order to achieve fast performance, here the Clock Gating structure is designed based on Transmission Gate Configuration. In conventional three stage comparator, the technology used is FinFET. Here, considering the same technology to develop proposed three stage comparator and its modified architecture. The entire designs are simulated using H-spice software and the comparison of conventional and proposed architectures in terms of power and delay are also presented. According to simulation results, the modified three stage comparator decreases power consumption by 20% it has a 17% energy efficiency.

Keywords: CMOS, FinFET, Dynamic Comparators, Input Referred Noise, Power Consumption, Tail Transistor

I. INTRODUCTION

Many applications such as signal filtering and processing are processed digitally. Designers of digital integrated circuit (IC) need to develop a fast analog to digital converter (ADC) circuit because ADC will influence the overall performance of the applications [1]. In these applications, the power consumption and processing time is very critical. Most ADCs use a comparator as part of their building blocks. Hence the comparator must have a high speed and consume less power. Comparator is used to compare two analog signals and will give the output in binary signal based on the comparison [2]-[3]. Since the input signals are usually low in amplitude, a preamplifier circuit is needed for the comparator. A differential amplifier with active loads is usually the first stage of the preamplifier. The differential amplifier will produce a very high gain. It amplifies the difference between two input voltages. The output of the preamplifier is connected to the decision-making circuit or latch. The decision-making circuit determines which signal is greater by comparing the signals. A flash and pipeline ADC architecture usually use the preamplifier based comparators [4]. A preamplifier based comparator is a regenerative comparator, it uses back to back latch stage and positive feedback [5, 6]. The preamplifier in a comparator with latch is used to reduce the kickback effect [1]-[5]. This will help in eliminating noise. A latch is defined as the memory unit that stores a charge on the gate capacitance of an inverter [4]. A commonly used architecture in analog circuits is a dynamic latch because it provides excellent speed along with an acceptable accuracy. A dynamic latch circuit can be constructed using a cross coupled pair of PMOS and NMOS transistors [6]-[7]. The latch works in two phases which is governed by a clock (CLK) level either low or high.

A. Latch Based Comparators:

Latch based comparators are used for low power design and high speed. The latch based comparator consists of 2 stages. The preamplifier stage of comparator improves the sensitivity of comparator from noise generated by feedback stage[2].The latch stage senses the small difference between the inputs and detects the larger input. The output buffer provides amplified outputs. An input referred latch offset voltage, resulting from threshold voltage VTH, current factor β (= μ COXW/L) and parasitic load capacitance mismatches, limits the accuracy of comparators [1]. The design of these stages is very important so as to achieve an efficient performance. In [3], double tail comparator it is proposed where the conventional comparator is changed for low power and quick operation as delay is reduced by adding few more transistors. Common mode input voltage is limited by low power operation. Comparators with high performance are required to amplify small inputs to signals with sufficient level to be detected by various systems [8]. In the proposed design of the comparator as in [1], a fully differential with an enhanced reset architecture using transmission gates to increase the speed has been used for sample and hold less ADC. A fast comparator with high accuracy is key element for ADC [9]. Apart from technological amendments, designing new circuits for low voltage operation and shunning stacking of transistors between the rails is preferred. In systems designed for testing and fault detection, window comparators are utilized. They are also required to meet the demand of low power design. The conventional window comparator [4]with voltage hysteresis property operating in noisy conditions employs comparators along with AND gate. Comparators are the vital elements of many electronic systems and it must be optimized to achieve higher performance.

B. Comparator:

In electronics, a comparator is used to compare two voltages and it will specify which input is higher by stating the output in digital form [1]. A block diagram of a comparator is illustrated in Figure 1. Two terminals at the input are the

analogue inputs indicated by V+ and V− and the output in digital form is Vo.

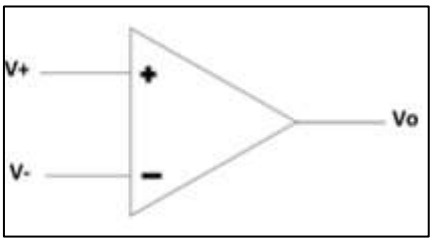


Fig. 1: Block diagram of a comparator

Referring to Figure 1, when the input voltage at the positive terminal (V+) is greater than the input voltage at the negative terminal (V-), the output will be a positive value or logic 1. However, when the input at the negative terminal is greater, the output voltage will be negative or logic 0.

C. Preamplifier:

The preamplifier is used to amplify the input signal. This is done by inputting the signal to the first stage of the preamplifier circuit which is a differential amplifier with active loads. This is followed by a circuit to minimize kickback noise and to reduce the effect of offset voltage error caused by of device mismatch [5]. The output of the preamplifier is connected to the decision-making circuit. The decision-making circuit compares the signals and determines which signal is greater. The output of the decision-making circuit is then converted into a logic signal [2] by an output buffer circuit. The preamplifier used here is self-biased differential circuit with active loads in order to reduce the effect of offset voltage error caused because of device mismatch [8].

D. Latch:

A dynamic latch stage is a second stage of the comparator circuit. In the circuit, two inverters connected back-to-back is used to form a differential comparator. NMOS transistors are also used and placed between the two differential nodes of the latch. The latch stage will amplify the difference between input signals after determining which of the input signals is greater. The output of the latch will be in digital output level indicating whether the differential input signal is positive or negative.

E. Finfet:

The basic structure of FinFET comprise of a silicon fin surrounded by shorted or independent gate on either side of the body, generally silicon insulator substrate. FinFET is comes with two gates which are operated independently or simultaneously. Here one gate is used to control the threshold voltage by using another gate voltage. In general the inclusion of FinFET devices are maximizing the system performance by suppressing the leakage current and power dissipation.

FinFET devices exhibit more drive current per unit area than planar devices, largely because the height of the fin can be used to create a channel with a larger effective volume but still take advantage of a wraparound gate. The added performance capability of FinFET can be used to achieve higher frequency numbers compared to bulk for a given power budget or lower power. The power reduction can come from two sources: reduced need for wide, high-drive standard cells; and the ability to operate with a lower supply voltage for a given amount of leakage.

F. TRANSMISSION GATE

In Transmission Gate parallel PMOS and NMOS devices are connected as bilateral CMOS switch. In general TG is symmetrical in nature in which input and output are completely interchangeable as compared to conventional CMOS logic. As shown in Figure 4.1 TG is comes with bilateral operation with the schematic of two superimposed triangles pointing in opposite directions.

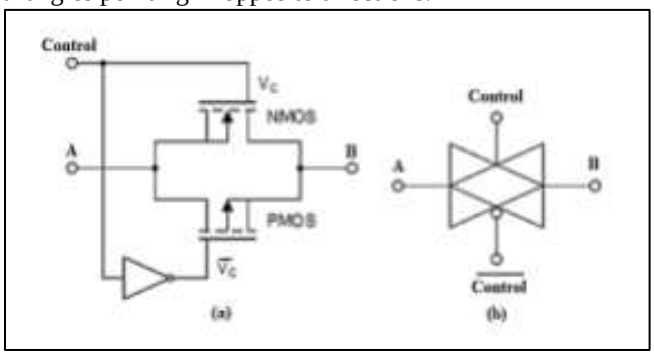


Fig. 2: (a) Circuit (b) Symbol

The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18-µm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced.

Summary: Although transistor count is more delay and power consumption are reduced.

II. EXISTING METHOD

As a result, it's required to evaluate whether the prior three step comparators' higher power usage is justified. As seen in Fig., Its outputs FN and FP connected to GND after the first-stage amplification. As a result, the gate–source voltage of the second-stage input pair M8–9 is equal to VDD. As a consequence, M8–M9 transistors current is strong enough to rapidly pull up RP and RN. As illustrated in Fig. , the tail transistor was introduced to the following step (latch) to minimize power usage. The circuit's functioning is as follows: Furthermore, in comparison to the Miyahara comparator's first-stage output load (M6–M7 transistors and M12–15 transistors in Fig.), the three-stage comparator's first-stage output load is only M8–M9 transistors in Fig. The output load is lowered by many orders of magnitude,

resulting in faster amplification. When compared to three stage comparators without a tail transistor, however, it improves amplification speed while lowering total power consumption.

First, rather than the first-stage output, the gate of M6–M7 transistors are shown in Fig. is linked to CLKB. The parasitic capacitance at the first-stage output is reduced as a result. Second, rather than being linked to the second-stage output, P3-gate is connected to CLK. The parasitic capacitance at the second-stage output is reduced as a result. Finally, the parasitic capacitance is reduced in initial stage. More crucially, it ensures that the M1–2 drain is at VDD at the start of the comparison. This is significant due to the input pair's saturation zone assists in the reduction of input referred noise.

The following circuit operates as follows. When CLK is 0 and CLKB is 1, during reset phase. The Fig. shows, RP1 and RN1 are set to GND, whereas the FP1 and FN1 are set to VDD. This disables N6, N8, and N9 in Fig , guaranteeing that the additional route N5-9 is free of static current. CLK climbs to 1 and CLKB falls to 0 during the amplification phase.

Fig. shows how RP1 and RN1 cause VDD. Then FN1 and FP1 become GND. The additional routes in Fig. 6 are switched on for a brief duration, since the RP1 and RN1 raising occurs before the FP1 and FN1 falling, a differential current is drawn from the latching nodes OUTN and OUTP.

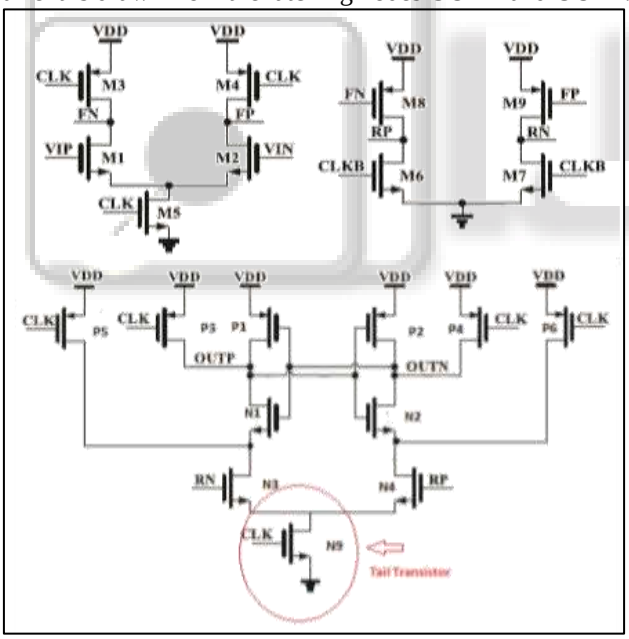


Fig. 3: Proposed three stage comparator

This creates a voltage difference between OUTN and OUTP, which speeds up regeneration phase while lowering comparator noise and input offset. The additional paths in Fig. 6 are switched off again once FN1 and FP1 connected to GND to prevent the static current. In this the extra tail transistor provides the less power consumption compared to three stage comparator.

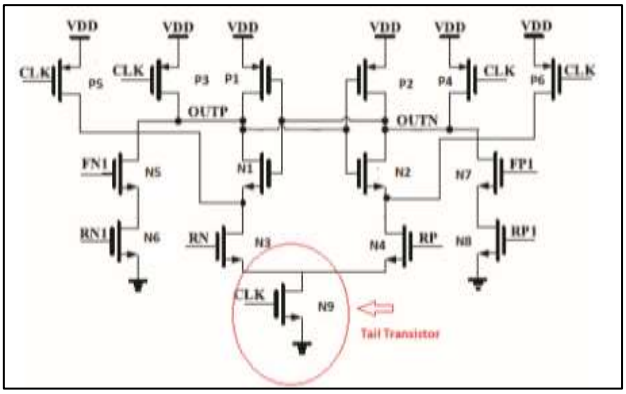


Fig. 4: © Modified three stage comparator

III. PROPOSED METHOD

In this paper, A three stage comparator is presented in a novel architecture. The methodology used for this architecture is Clock Gating technique. In order to achieve fast performance, here the Clock Gating structure is designed based on Transmission Gate Configuration.

A. Clock Gating Technique.

The clock gating technique requires an extra logic to generate a clock enabling signal and this will be enabled only when they attain logic 0 or 1 value according to the circuit design, which leads to reduction in either power or delay based on the circuits.

B. Gate based clock gating

One of the simplest techniques is the gate-based clock gating where the design is simple and easy for implementation. In this technique any of the gates can be used. The discussed gates are AND gate, OR gate and NOR gate.

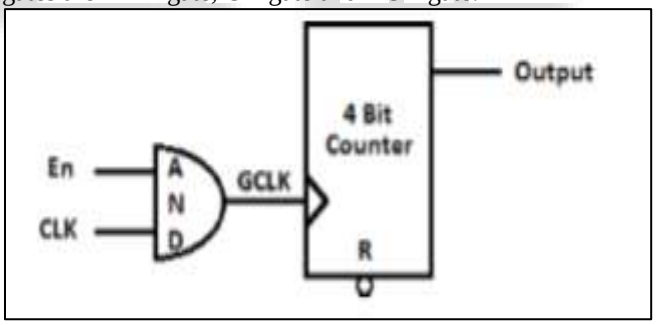


Fig. 5: And Based Clock Gating Technique

C. Schematic of And Gate using Transmission Gate Logic:

As seen in the introduction of Transmission Gate Logic, there exists one control input which acts as complementary inputs for both PMOS and NMOS transistors in parallel and one input. To design AND Gate in Transmission Gate Logic, here considering the input as A and control input as B. The following figure show the structure of AND Gate:

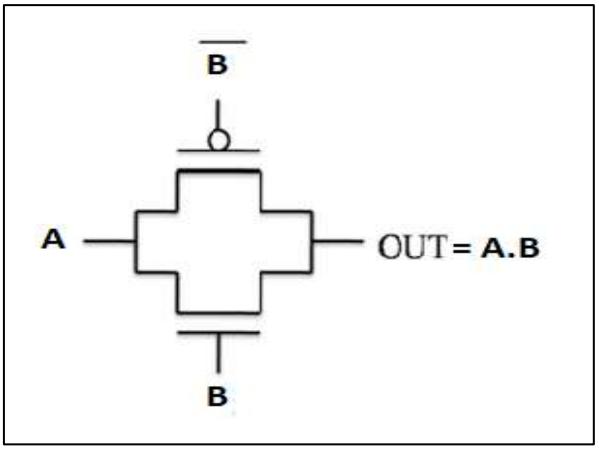


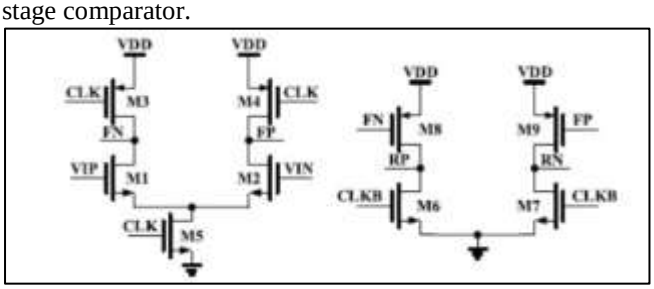
Fig. 6: Circuit of AND Gate using Transmission Gate Logic

Here considering the input as EN and control input as CK, the output is considered as the CLK in implementing proposed three stage comparator. From the above figures, it is shown that the structure of three stage comparators using transmission gate-based clock gating techniques is describes as follow. The operation of these proposed schematics is already described in previous chapter. In these proposed schematics, the clock signal is applied through an AND gate which output is fed as a clock signal to three stage comparators.

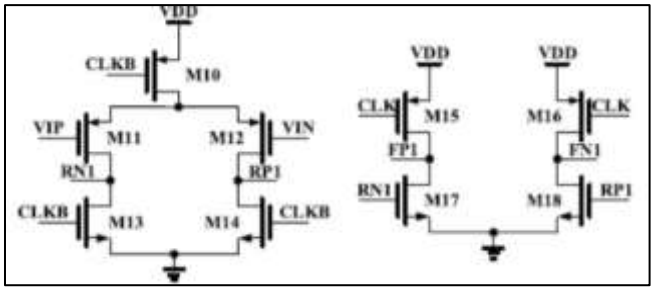
IV. MODIFIED THREE STAGE COMPARATORS WITH TAIL TRANSISTOR

As a result, it's required to evaluate whether the prior three step comparators' higher power usage is justified. As seen in Fig. 3, Its outputs FN and FP connected to GND after the first-stage amplification. As a result, the gate–source voltage of the second-stage input pair M8–9 is equal to VDD. As a consequence, M8–M9 transistors current is strong enough to rapidly pull up RP and RN. As illustrated in Fig. 5, the tail transistor was introduced to the following step (latch) to minimize power usage. The circuit's functioning is as follows: Furthermore, in comparison to the Miyahara comparator's first-stage output load (M6–M7 transistors and M12–15 transistors in Fig. 1), the three-stage comparator's first-stage output load is only M8–M9 transistors in Fig. 3.

The output load is lowered by many orders of magnitude, resulting in faster amplification. When compared to threestage comparators without a tail transistor, however, it improves amplification speed while lowering total power consumption. Fig.4 (d) shows the transient response of 3-stage comparator.



(a)



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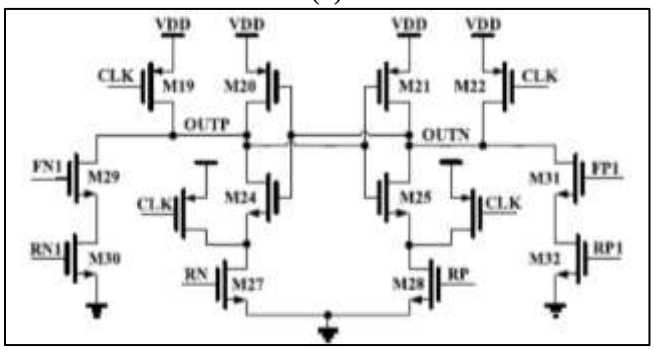
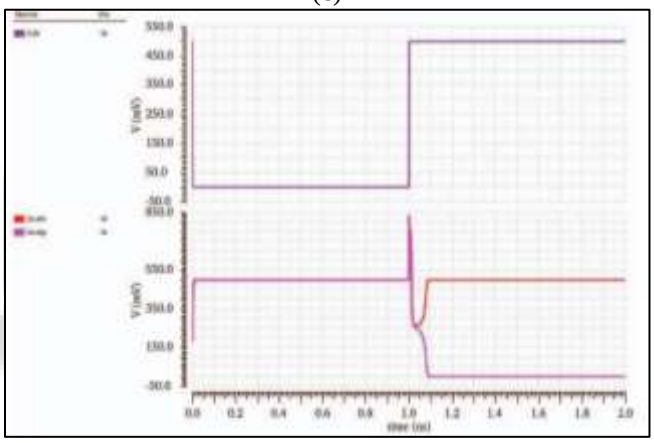


(c)



(d)

Fig. 7: 3-stage comparator. (a) 2-stages of preamplifiers with nMOS pair. (b) another 2-stages of preamplifiers with pMOS pair. (c) latch stage [13] (d) Transient response.

The three-stage comparator's transient simulation is shown in Figure 5 (b) at 1mV voltage difference in between input pair. First, rather than the first-stage output, the gate of M6–M7 transistors are shown in Fig. 3 is linked to CLKB. The parasitic capacitance at the first-stage output is reduced as a result. Second, rather than being linked to the second-stage output, P3-gate is connected to CLK. The parasitic capacitance at the second-stage output is reduced as a result. Finally, the parasitic capacitance is reduced in initial stage. More crucially, it ensures that the M1–2 drain is at VDD at the start of the comparison. This is significant due to the input pair's saturation zone assists in the reduction of input referred noise.

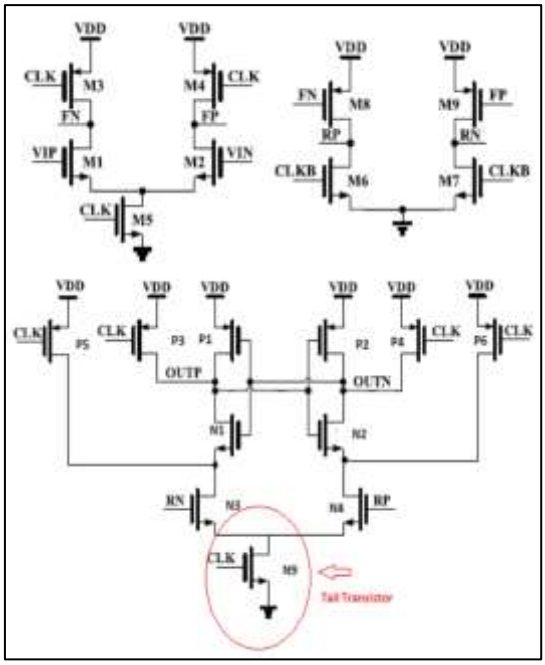


Fig. 5: (a). Modified three stage comparator of Fig.3 with tail transistor

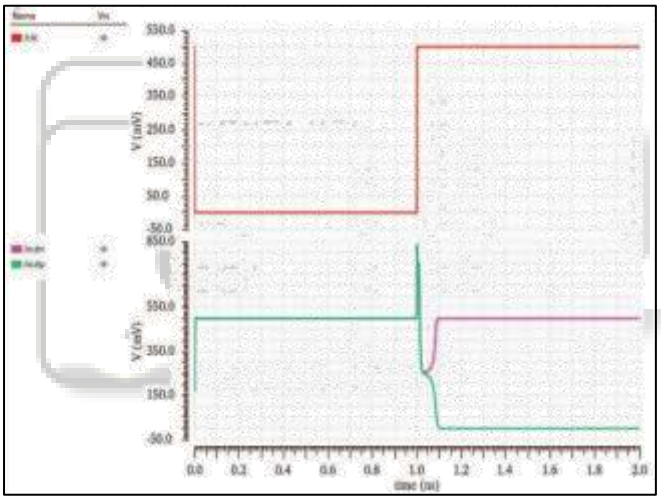


Fig. 5: (b) Transient response of three stage comparator with tail transistor

When the tail transistor is used in the latch stage, there is no static path between VDD and GND when CLK='0,' which reduces power consumption and improves the overall energy efficiency of the comparator. As seen in Fig 5(c), increasing the tail transistor width reduces the amplification delay. As illustrated in Fig.6, the tail transistor was also added to the three-stage comparator (Fig. 4).

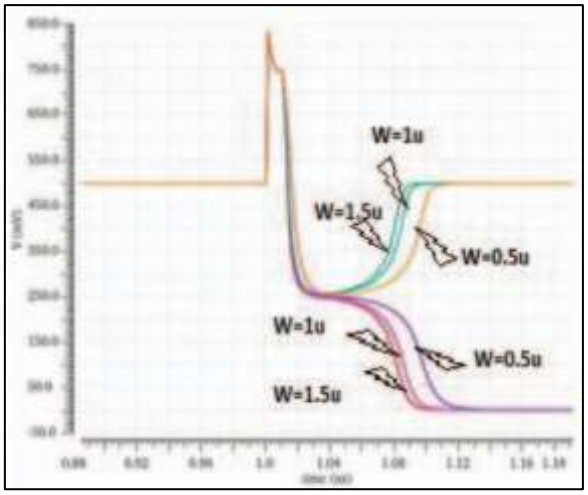


Fig. 5: (c) Transient response of three stage comparator with tail transistor.

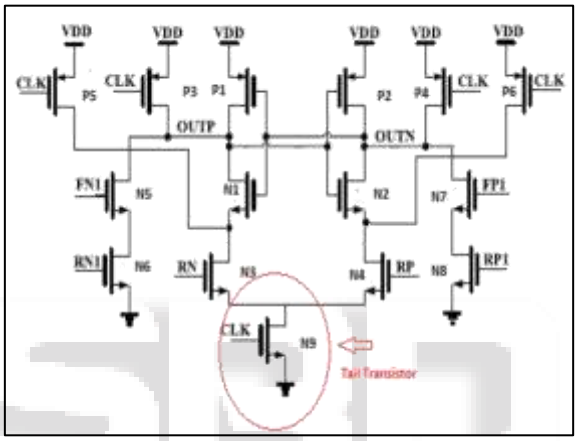


Fig.6(a). Modified three stage comparator of Fig.4 with tail transistor

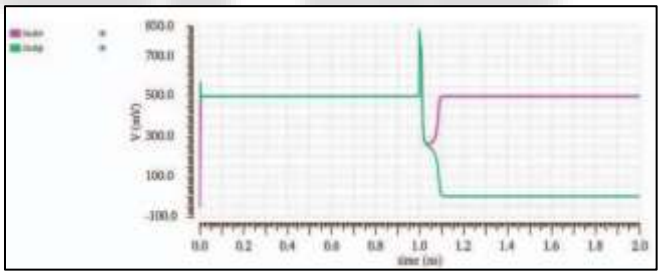


Fig. 6(b) Transient response of three stage comparator (Fig.4) with tail transistor

The following circuit operates as follows. When CLK is 0 and CLKB is 1, during reset phase. The Fig. 4 shows, RP1 and RN1 are set to GND, whereas the FP1 and FN1 are set to VDD. This disables N6, N8, and N9 in Fig. 6, guaranteeing that the additional route N5-9 is free of static current. CLK climbs to 1 and CLKB falls to 0 during the amplification phase. Fig. 6 shows how RP1 and RN1 cause VD

TABLE II COMPARISONS OF THE THREE STAGE COMPARATORS WITH AND WITHOUT TAIL TRANSISTOR

Input Voltage Difference	3-stage comparators without tail transistor						3-stage comparator with tail transistor					
	Fig.3			Fig.4.			Fig.5.			Fig.6.		
	Power (uW)	Delay (pS)	Energy (fJ)	Power (uW)	Delay (pS)	Energy (fJ)	Power (uW)	Delay (pS)	Energy (fJ)	Power (uW)	Delay (pS)	Energy (fJ)
1mV	1.92	80	0.154	2.65	73	0.19	1.55	82	0.13	2	85	0.17
5mV	1.9	68	0.130	2.65	58	0.15	1.55	70	0.11	1.99	70	0.14
10mV	1.9	56	0.11	2.67	46	0.12	1.53	60	0.09	1.99	60	0.12
20mV	1.89	44	0.083	2.7	30	0.08	1.51	44	0.06	2.1	50	0.11
40mV	1.89	36	0.068	2.8	30	0.084	1.5	36	0.05	2.15	32	0.07
60mV	1.88	32	0.06	3	30	0.09	1.5	32	0.045	2.35	30	0.07
80mV	1.87	30	0.059	3.1	27	0.083	1.5	28	0.04	2.4	28	0.07
100mv	1.85	30	0.055	3.1	25	0.077	1.5	28	0.04	2.45	28	0.07

V. RESULTS AND DISCUSSION

This section contrasts the proposed three-stage comparators with the conventional there-stage comparators without tail transistor. The design of all comparators is also used the same transistor aspect ratio (1u/20nm), so that other specifications can be compared. Table II provides the contrast of this work with the conventional designs.

Table II presents, the power consumption of 3-stage comparators with tail transistor is smaller than the 3-stage comparators without tail transistor by 20%, 24.5% of Fig.3 and Fig.4 respectively. Meanwhile, the delay of 3-stage comparators with tail transistor is higher than the 3-stage comparators without tail transistor by 2.4%, 14% of Fig.3 and Fig.4 respectively. The energy efficiency of 3-stage comparators with tail transistor is higher than the 3-stage comparators without tail transistor by 17%, 10% of Fig.3 and Fig.4 respectively.

Width (um)	3-stage comparator with tail transistor					
	Fig.5.			Fig.6.		
	Power (uW)	Delay (pS)	Energy (fJ)	Power (uW)	Delay (pS)	Energy (fJ)
0.5	1.54	87	0.14	1.99	89	0.18
1	1.55	82	0.13	2	85	0.17
1.5	1.56	75	0.11	2.1	78	0.16

Table 3: comparisons of the three stage comparators with various widths of tail transistor

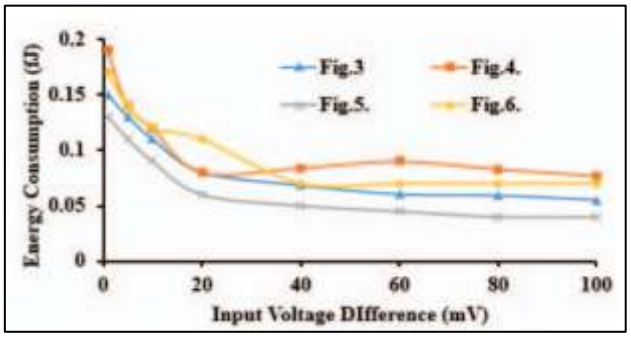
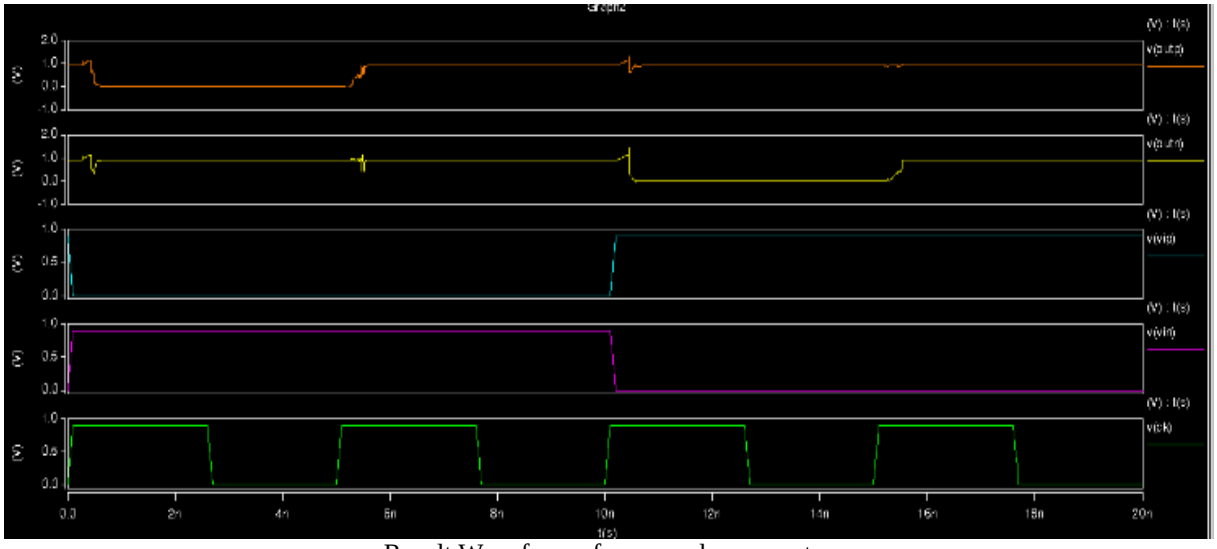


Fig. 7: shows the Energy consumption of different three stage comparators. Table III represents the power, delay and energy of three stage comparators with various widths of tail transistor at 1mV input voltage difference.

	DELAY	POWER
Existing	5.2013ns	24.228nW
MODIFIED Existing	5.183ns	47.828nW
Proposed	0.263ns	34.21nW
MODIFIED PROPOSED	0.4386ns	54.5nW

Table 4: Evaluation of power, delay, area parameters



Result Waveform of proposed comparator

VI. CONCLUSION:

This brief presents a three-stage comparator and its modified version using clock gating technique in transmission gate logic, which have the advantages of fast speed, low kickback noise. These comparators are well suited for high-speed high-resolution SAR ADCs. Finally, measured results validate the effectiveness of these comparators. All the design are implemented in H-spice using Finfet technology.

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